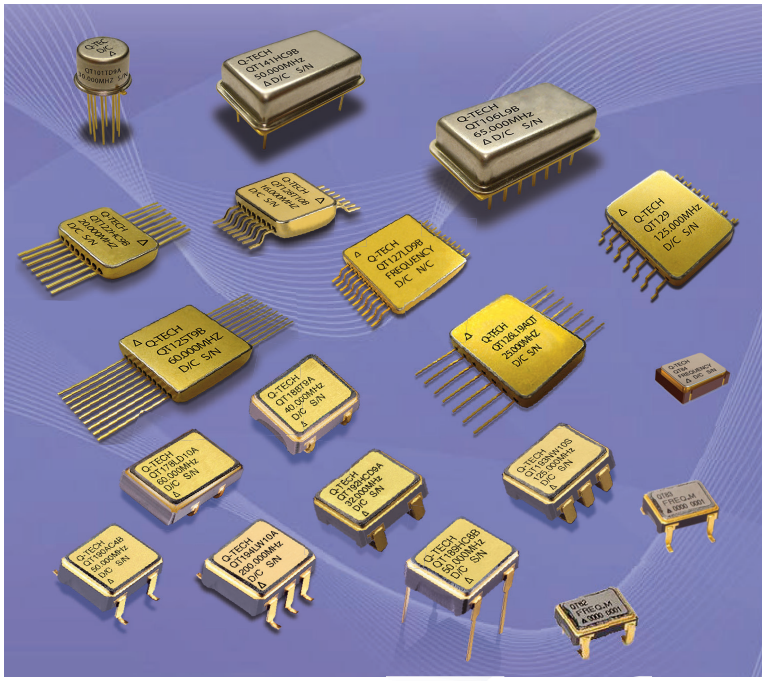
Q-TECH CORPORATION

CLASS B+ PRODUCTS

HIGH RELIABILITY HYBRID CRYSTAL CLOCK OSCILLATORS

1.8 to 5.0Vdc - 15kHz to 250MHz



Features

- Made in the USA - ECCN: EAR99
- DFARS 252-225-7014 Compliant Electronic Component Exemption
- Broad frequency range from 15kHz to 250MHz (for higher frequencies please consult the factory)
- Rugged 4-point mount (SMD ceramic) or 3 point mount (others) shock resistant
- Small packages and footprints offering 5x7mm SMT and leaded with 4-point crystal mount
- 100kRad (Si) tolerant
- ACMOS, LVCMOS, TTL, LVDS, LVPECL
- Tristate Output option (-D) except for LVDS and LVPECL (standard)
- Hermetically sealed package
- Fundamental and 3rd Overtone design
- Swept Quartz Crystal or Cultured Quartz Crystal
- Low phase noise and jitter
- Q-Tech does not use pure lead or pure tin in its products
- Custom screening and QCI available with MCM part number
- MIL-PRF-55310/9, /16, /21, /26, /27, /28, /30, /33, /34, /35, /36, /37, /38, /39, /40 equivalent

Ordering Information

(Sample part number)

QT188ACD10S-100.000MHz

Q	T	1	88	AC	D	10	S	-	100.000MHz

Lead Finish:

T	= Standard (*)
S	= Solder Dip (**)

Materials Level

1	= 100kRad Tolerant Die, Swept Quartz Crystal
2	= 100kRad Tolerant Die, Cultured Quartz Crystal
3	= Class B Die, Swept Quartz Crystal

Package:

See Pages 5-7, 29-32

Logic & Supply Voltage:

(All B+ Packages)			
AC	=	ACMOS (****)	5.0V
HC	=	HCMOS	5.0V
T	=	TTL	5.0V
L	=	LVCMOS	3.3V
N	=	LVCMOS	2.5V
R	=	LVCMOS	1.8V
(QT122, QT128, QT125, QT127, QT129, QT130, QT180, QT185, QT186, QT187, QT193 & QT194 Only)			
LW	=	LVDS	3.3V
NW	=	LVDS	2.5V
LP	=	LVPECL	3.3V
NP	=	LVPECL	2.5V

Tristate Option:
See Note (*****)

Blank	= No Tristate
D	= Tristate

Output Frequency

Screening Option:

S	= Per MIL-PRF-38534, Class K (modified)
A	= Per MIL-PRF-55310, Level S
C	= Per MIL-PRF-55310, Level S (modified)
B	= Per MIL-PRF-55310, Level B (modified)
N	= Per NASA EEE-INST-002, Level 1
E	= Engineering Model

Note: If breadboard model is desired, refer to normal QT products or consult with Q-Tech.

Frequency vs. Temperature Code (***):

2	= ±	65ppm at -55ºC to +125ºC
6	= ±	50ppm at -55ºC to +105ºC
7	= ±	75ppm at -55ºC to +125ºC
9	= ±	50ppm at -55ºC to +125ºC (***)
10	= ±	100ppm at -55ºC to +125ºC
11	= ±	50ppm at -40ºC to +85ºC
12	= ±	100ppm at -40ºC to +85ºC
16	= ±	100ppm at -55ºC to +105ºC
19	= ±	15ppm at 23ºC ± 1ºC (***) 50ppm at -55ºC to +125ºC reference to F at 23ºC

(*) Gold Plated: 50µ ~ 80µ inches typ.

(**) Hot Solder Dip Sn60/Pb40 per MIL-PRF 55310 is optional for an additional cost

(***) Frequency stability vs. temperature codes may not be available in all frequencies. For 5x7mm products, Code 19 is only available for ≤32MHz and Code 9 is only available for ≤100MHz.

(****) HCMOS & TTL compatible

(*****) (D) code for tristate is not required for LW, NW, LP and NP logic types. This enable/disable function is included by default.

For Non-Standard requirements, contact Q-Tech Corporation at Sales@Q-Tech.com

GENERAL SPECIFICATION

1 SCOPE

1.1 Scope. This specification establishes the general quality and reliability requirements for a family of hybrid, hermetically sealed square wave, B+ crystal oscillators.

1.2 Part Number. The part number shall be as specified in the detail specification.

2 APPLICABLE DOCUMENTS

2.1 Specifications and Standards. Unless otherwise specified, the following documents shall be applicable to this specification to the extent specified herein.

SPECIFICATIONS

MIL-PRF-55310 Crystal Oscillators, General Specification For

MIL-PRF-38534 Hybrid Microcircuits, General Specification For

EEE-INST-002 Instructions for EEE Parts Sections, Screenings, Qualifications and Ratings

STANDARDS

MIL-STD-202 Test Methods for Electronic and Electrical Component Parts

MIL-STD-883 Test Methods and Procedures for Microelectronics

2.2 Conflicting Requirements. In the event of conflict between requirements of this specification and other requirements of the applicable detail drawing, the precedence in which requirements shall govern, in descending order, is as follows:

a) Applicable Customer purchase order.

b) Applicable Customer detail drawing.

c) This specification.

d) Other specifications or standards referenced in 2.1 herein.

2.3 Customer Purchase Order Special Requirements. Additional special requirements shall be specified in the applicable Customer purchase order when additional requirements or modifications specified herein are needed for compliance to special program or product line requirements

3 REQUIREMENTS

3.1 Item Requirements. The individual item requirements shall be as specified herein and the detail specification.

3.2 Case Outline. The case outline shall be as specified in the detail specification. (See pages 29 to 32).

3.2.1 Terminal Connections. The terminal connections shall be as shown on page 33.

3.2.2 Lead Material and Finish. Lead material and finish shall be as shown on page 34.

3.2.3 Hot Solder Dip. Terminals can be solder dipped Sn60/Pb40 per MIL-PRF-55310 at additional cost. Prefix designated with an “S”. See sample part number in the “Ordering Information” table.

3.2.4 Solderability. Leads shall meet the requirements of MIL-PRF-55310/38534 when tested.

3.3 Maximum Ratings. Unless otherwise specified, the maximum ratings shall as specified in the detail specification.

3.4 Electrical Performance Requirements. The electrical performance requirements shall be as specified herein and the applicable detail specification.

3.5 Design and Construction. The design and construction of the crystal oscillator shall be as specified herein. As a minimum, the oscillators shall meet the design and construction requirements of MIL-PRF-55310.

GENERAL SPECIFICATION (Cont'd)

3.5.1 Construction Technology. The device shall be constructed as a class 2-Type 1 hybrid oscillator of MIL-PRF-55310.

3.5.2 Workmanship. The device workmanship shall meet the requirements of MIL-PRF-55310.

3.5.3 Element Derating. All active and passive elements shall be derated in accordance with the applicable hybrid microcircuit element requirements of MIL-STD-975. Elements shall not operate in excess of derated values.

3.5.4 Active Elements. The active component shall be derived from lots that meet the Element Evaluation requirements of MIL-PRF-38534, Class K (for QT100 and QT200), 100kRad (Si) tolerant, and MIL-PRF-55310, Level B (QT300).

3.5.4.1 Scanning Electron Microscopy.
There is a potential of metallization thinning per MIL-STD-883, Method 2018 that can be observed during DPA for active die using 0.8µm BiCMOS technology. The active die in this series are CMOS, LVDS, and LVPECL with frequencies between 70MHz and 250MHz for 1.8Vdc, 2.5Vdc, and 3.3Vdc supply.

The requirement per MIL-STD-883, Method 2018 is for multi-directional contacts. For contacts with >10% wrap around, the metallization shall be ≥20%. The worst step coverage either in Metal 1 (M1) or Metal 2 (M2) without barrier may see a result of less than 20% during DPA work of cross-sectioning.

There is a concern of how the preparation for SEM was performed since the oxide film around the metal is etched back and anti-reflection film was removed. The DPA work uses a chemical wet etch method that could cause the SiO_2 layer and poly-silicon under Metal 1 (M1) of the DPA unit to melt away during the chemical process and prior to SEM examination.

Although the worst-step coverage is less than 20% per MIL-STD-883, Method 2018, the calculation of current density met the requirement of $2x10^5$ A/cm^2 applicable to conductors of 99.99% Aluminum per MIL-PRF-38535, Appendix A and is not a concern in reliability and quality of the oscillators. Worst step coverage can be accepted at 12% or higher to maintain the current density as calculated.

3.5.5 Quartz Crystal. Unless otherwise specified by the detail specification, the quartz crystal material for the QT100 and QT300 shall be swept synthetic, grade 2.2 millions or better and cultured quartz crystal for QT200.

3.5.6 Passive Elements. Element Evaluation shall be as a minimum in accordance with MIL-PRF-55310, Level S for QT100 and Level B for QT200 And QT300.

3.5.7 Crystal Mounting. The crystal element shall be three-point minimum mounted in such a manner as to assure adequate crystal performance when the oscillator is subjected to the environmental conditions specified herein.

3.5.8 Maximum Allowable Leak Rate. The maximum allowable leakage rate shall be as specified by MIL-STD-883, method 1014 based on the internal cavity volume. The hermetic seal (fine and gross leak) tests shall be in accordance with MIL-STD-883, Method 1014, with Leak Rate $5x10^{-8}$ atm-cm^3/s Helium gas unless otherwise specified.

3.5.9 Weight. The maximum weight of the crystal oscillator shall be defined on page 34.

3.5.10 Delta Criteria. The crystal oscillator shall meet the parameter delta criteria post burn-in called out in the detail specification. The change in the parameter (delta) shall be calculated between the initial measurement and the present (interim or final) measurement.

3.5.11 Marking. Each unit shall be permanently marked with the manufacturer's name or symbol, part number, frequency, lot date code number, and serial number. The unit shall be marked with the outline of an equilateral triangle near pin 1 to show that it contains devices which are sensitive to electrostatic discharge.

3.5.12 Traceability. Material, element and process traceability requirements shall be as specified by MIL-PRF-55310.

3.5.13 Rework Provisions. Rework shall be in accordance with the provisions of MIL-PRF-55310.

4 QUALITY ASSURANCE PROVISIONS

4.1 Responsibility for Inspection. Unless otherwise specified in the contract or purchase order, the supplier shall be responsible for the performance of all inspection requirements as specified. Customer reserves the right to perform any of the inspections set forth in the specification where such inspections are deemed necessary to assure supplies and services conform to prescribed requirements, and to return any product failing to meet the specified requirements.

GENERAL SPECIFICATION (Cont'd)

4.2 Screening. Hybrid crystal oscillators shall have been subjected to and successfully passed all the screening tests as applicable in Tables I, II, III, IV, V, VI.

4.2.1 Nondestructive Bondpull. 100% Non-destructive bondpull applicable to screening S, A, C, N.

4.2.2 Percent Defective Allowable (PDA). The percent defective allowable shall be 2% (Screening Option S, A, C) or 5% (Screening Option N) 10% (Screening Option B) or one device, whichever is greater. PDA accountability shall be based on failures occurring during the second half of burn-in only. PDA shall be applicable to the +25 ºC static parameters as specified in the delta criteria.

4.3 Quality Conformance Inspection (QCI). Shall be as outlined in the QCI section for each screening option here-in. All records shall be traceable to the lot number and unit serial number. Samples used for Group A that pass all tests may be delivered on contract prior to QCI completion.

4.4 Customer Source Inspection. Provisions for periodic in-process source inspection by Customer shall be included in the supplier's manufacturing plan. Q-Tech will notify customer when the deliverable devices are ready for an in-process source inspection. The inspection points shall, as a minimum, be:

a) Pre crystal mount visual inspection.

b) Post crystal mount visual inspection (before final Au adjust).

c) Prior to shipment inspection.

4.5 Retention of Records. All records pertaining to the design, processes, incoming receiving, in-process inspections, screening and quality conformance inspection, product lot identification, product traceability, failure reports and analyses etc., shall be retained by the vendor for a period of seven years from the date of product shipment.

5 PREPARATION FOR DELIVERY

5.1 Packaging. The requirements for packaging shall be in accordance with MIL-PRF-55310.

5.2 Electrostatic Discharge Sensitivity. Meet MIL-STD-883, Method 3015, Class 1C HBM

6 NOTES

6.1 Ordering Data. The contract or purchase order should specify the following:

a) Customer or Q-Tech part number.

b) Quality Conformance Inspection requirements.

c) Requirements for special technical documentation.

d) Test data requirements.

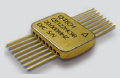
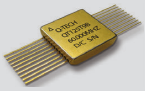
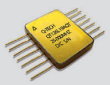
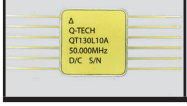
e) Special packaging.

f) Requirement for source inspection and notification.

6.2 Handling. The devices used must be handled with certain precautions to avoid damage due to electrostatic discharge.

6.3 Certificate of Conformance. Deliverables include a certificate of conformance to this specification, signed by an authorized representative of the manufacturer.

CLASS B+ PRODUCT OFFERINGS

Photo	Product QT	Package	Output Logic	Vdd (V)	Frequency Range	Outline	Pin Connection
	QT101 QT201 QT301	Transistor Outline (TO-5) 8 Pin	CMOS TTL	1.8Vdc, 2.5Vdc, 3.3Vdc, 5.0Vdc	450kHz to 85MHz	Page 29	Page 33
	QT106 QT206 QT306	Dual In-Line (DIP-14) 14 Pin	CMOS TTL	1.8Vdc, 2.5Vdc, 3.3Vdc, 5.0Vdc	15kHz to 200MHz		
	QT141 QT241 QT341	Dual In-Line (DIP-14) 4 Pin	CMOS TTL	1.8Vdc, 2.5Vdc, 3.3Vdc, 5.0Vdc	15kHz to 200MHz		
	QT142 QT242 QT342	Dual In-Line (DIP-14) 4 Pin	CMOS TTL	1.8Vdc, 2.5Vdc, 3.3Vdc, 5.0Vdc	15kHz to 200MHz		
	QT122 QT222 QT322	Flat Pack (FP) 16 Pin	CMOS TTL LVDS LVPECL	1.8Vdc, 2.5Vdc, 3.3Vdc, 5.0Vdc	450kHz to 250MHz	Page 30	
	QT128 QT228 QT328	Flat Pack (FP) 16 Pin Formed Lead	CMOS TTL LVDS LVPECL	1.8Vdc, 2.5Vdc, 3.3Vdc, 5.0Vdc	450kHz to 250MHz		
	QT125 QT225 QT325	Flat Pack (FP) 20 Pin	CMOS TTL LVDS LVPECL	1.8Vdc, 2.5Vdc, 3.3Vdc, 5.0Vdc	15kHz to 250MHz		
	QT127 QT227 QT327	Flat Pack (FP) 20 Pin Formed Lead	CMOS TTL LVDS LVPECL	1.8Vdc, 2.5Vdc, 3.3Vdc, 5.0Vdc	15kHz to 250MHz		
	QT126 QT226 QT326	Flat Pack (FP) 14 Pin	CMOS TTL LVDS	1.8Vdc, 2.5Vdc, 3.3Vdc, 5.0Vdc	15kHz to 250MHz		
	QT129 QT229 QT329	Flat Pack (FP) 14 Pin Formed Lead	CMOS TTL LVDS	1.8Vdc, 2.5Vdc, 3.3Vdc, 5.0Vdc	15kHz to 250MHz		
	QT130/QT131 QT230/QT231 QT330/QT331	Flat Pack (FP) 12 Pin	CMOS TTL LVDS LVPECL	1.8Vdc, 2.5Vdc, 3.3Vdc, 5.0Vdc	15kHz to 250MHz		

Notes:

1. LVDS and LVPECL are only available in 2.5V and 3.3V.
2. TTL is only available in 5.0V.
3. Not all frequencies ranges listed are available for all logic types. See Pages 20 - 24 for available frequencies for each logic type/package.

CLASS B+ PRODUCT OFFERINGS

Photo	Product QT	Package	Output Logic	Vdd (V)	Frequency Range	Outline	Pin Connection
	QT178 QT278 QT378	Surface Mount (SMD) 4 Pin J-Lead	CMOS TTL	1.8Vdc, 2.5Vdc, 3.3Vdc, 5.0Vdc	15kHz to 162.5 MHz	Page 31 & 32	Page 33
	QT188 QT288 QT388	Surface Mount (SMD) 4 Pin J-Lead	CMOS TTL	1.8Vdc, 2.5Vdc, 3.3Vdc, 5.0Vdc	450kHz to 162.5 MHz		
	QT189 QT289 QT389	4 Pin Thru-hole	CMOS TTL	1.8Vdc, 2.5Vdc, 3.3Vdc, 5.0Vdc	450kHz to 162.5 MHz		
	QT190 QT290 QT390	Surface Mount (SMD) 4 Pin Gull Wing	CMOS TTL	1.8Vdc, 2.5Vdc, 3.3Vdc, 5.0Vdc	450kHz to 162.5 MHz		
	QT192 QT292 QT392	Surface Mount (SMD) 4 Pin Formed Lead	CMOS TTL	1.8Vdc, 2.5Vdc, 3.3Vdc, 5.0Vdc	450kHz to 162.5 MHz		
	QT193 QT293 QT393	Surface Mount (SMD) 6 Pin Formed Lead	CMOS TTL LVDS LVPECL	1.8Vdc, 2.5Vdc, 3.3Vdc, 5.0Vdc	450kHz to 250 MHz		
	QT194 QT294 QT394	Surface Mount (SMD) 6 Pin Gull Wing	CMOS TTL LVDS LVPECL	1.8Vdc, 2.5Vdc, 3.3Vdc, 5.0Vdc (Note 1)	450kHz to 250 MHz		

Notes:

1. LVDS and LVPECL are only available in 2.5V and 3.3V.
2. TTL is only available in 5.0V.
3. Not all frequencies ranges listed are available for all logic types. See Pages 20 - 24 for available frequencies for each logic type/package.

CLASS B+ PRODUCT OFFERINGS

Photo	Product QT	Package	Output Logic	Vdd (V)	Frequency Range	Outline	Pin Connection
	QT184 QT284 QT384	5x7mm Surface Mount (SMD) 4 Pads	CMOS TTL	1.8Vdc, 2.5Vdc, 3.3Vdc, 5.0Vdc	500kHz to 162.5 MHz	Page 31 & 32	Page 33
	QT181 QT281 QT381	5x7mm 4 Pin Thru-hole	CMOS TTL	1.8Vdc, 2.5Vdc, 3.3Vdc, 5.0Vdc	500kHz to 162.5 MHz		
	QT182 QT282 QT382	5x7mm Surface Mount (SMD) 4 Pin Formed Lead	CMOS TTL	1.8Vdc, 2.5Vdc, 3.3Vdc, 5.0Vdc	500kHz to 162.5 MHz		
	QT183 QT283 QT383	5x7mm Surface Mount (SMD) 4 Pin Gull Wing	CMOS TTL	1.8Vdc, 2.5Vdc, 3.3Vdc, 5.0Vdc	500kHz to 162.5 MHz		
	QT185 QT285 QT385	5x7mm Surface Mount (SMD) 6 Pads	CMOS LVDS LVPECL	1.8Vdc, 2.5Vdc, 3.3Vdc, 5.0Vdc	80MHz to 162.5MHz	Page 31 & 32	
	QT186 QT286 QT386	5x7mm 6 Pin Thru-hole	CMOS LVDS LVPECL	1.8Vdc, 2.5Vdc, 3.3Vdc, 5.0Vdc	80MHz to 162.5MHz		
	QT187 QT287 QT387	5x7mm Surface Mount (SMD) 6 Pin Formed Lead	CMOS LVDS LVPECL	1.8Vdc, 2.5Vdc, 3.3Vdc, 5.0Vdc	80MHz to 162.5MHz		
	QT180 QT280 QT380	5x7mm Surface Mount (SMD) 6 Pin Gull Wing	CMOS LVDS LVPECL	1.8Vdc, 2.5Vdc, 3.3Vdc, 5.0Vdc	80MHz to 162.5MHz		

Notes:

1. LVDS and LVPECL are only available in 2.5V and 3.3V.
2. TTL is only available in 5.0V.
3. Not all frequencies ranges listed are available for all logic types. See Pages 20 - 24 for available frequencies for each logic type/package.

SCREENING OPTIONS SUMMARY

Test Description	Screening S Modified MIL-PRF-38534 Class K See Details in Table I (Pages 9 - 10)	Screening A MIL-PRF-55310 Level S See Details in Table II (Page 11 - 12)	Screening C Modified MIL-PRF-55310 Level S See Details in Table III (Page 13 - 14)	Screening N EEE-INST-002 Level 1 See Details in Table IV (Page 15 - 16)	Screening B Modified MIL-PRF-55310 Level B See Details in Table V (Page 17 - 18)	Screening E Engineering Model See Details in Table VI (Page 19)
Non Destructive Bond Pull	✓	✓	✓	✓	N/A	N/A
Internal Visual	✓	✓	✓	✓	✓	✓
Stabilization Bake	✓	✓	✓	✓	✓	✓
Random Vibration	N/A	✓	✓	N/A	N/A	N/A
Thermal Shock	N/A	✓	✓	✓	N/A	N/A
Temperature Cycling	✓	✓	✓	✓	✓	N/A
Constant Acceleration	✓	✓	✓	✓	✓	N/A
Particle Impact Noise Detection (PIND)	✓	✓	✓	✓	✓	N/A
Pre Burn-In Electrical	✓	✓	✓	✓	✓	N/A
Burn-In # 1	✓ (160 Hrs at +125ºC)	✓ (240 Hrs at +125ºC)	✓ (240 Hrs at +125ºC)	✓ (240 Hrs at +125ºC)	✓ (160 Hrs at +125ºC)	N/A
Interim Electrical	✓	N/A	N/A	N/A	N/A	N/A
Burn-In # 2	✓ (160 Hrs at +125ºC)	N/A	N/A	N/A	N/A	N/A
Final Electrical	✓	✓	✓	✓	✓	✓
Percent Defective Allowance (PDA)	✓	✓	✓	✓	✓	N/A
Seal Fine Leak	✓	✓	✓	✓	✓	✓
Seal Gross Leak	✓	✓	✓	✓	✓	✓
Radiographic Inspection	✓	✓	N/A	N/A	N/A	N/A
Frequency Aging 30 days	✓	100% Group B Tested	N/A	✓	(QCI Group B)	N/A
External Visual	✓	✓	✓	✓	✓	✓
Group A Inspection (QCI)	✓ See Details in Table I-c	✓ MIL-PRF-55310 Level S	✓ MIL-PRF-55310 Level S	✓ EEE-INST-002 Level 1	✓ MIL-PRF-55310 per Table V-b	N/A
Group B Inspection (Aging)	N/A (aging performed in screening)	✓ MIL-PRF-55310 Level S	N/A	N/A (aging performed in screening)	MIL-PRF-55310 (Optional)	N/A

Note: If breadboard model is desired, refer to normal QT products or consult with Q-Tech.

Screening - Option S (Modified MIL-PRF-38534, Class K)

(Example: QT178LD10S-50.000MHz)

Table I

Test Description	MIL Standard	Method	Condition	Qty	Comments
Non Destructive Bond Pull	883	2023		100%	Completed During Assembly
Internal Visual	883	2017	Class K	100%	
Stabilization Bake	883	1008	C 48 hours at +150°C	100%	
Temperature Cycling	883	1010	C	100%	10 cycles
Constant Acceleration	883	2001	A	100%	Y1 direction only (5,000g's)
Particle Impact Noise Detection (PIND)	883	2020	B	100%	
Pre Burn-In Electrical	Refer to Table I-b and Detail Specifications			100%	
Burn-In # 1	883	1015	+125°C for 160 hours	100%	With load and nominal supply voltage
Interim Electrical	Refer to Table I-b and Detail Specifications			100%	
Burn-In # 2	883	1015	+125°C for 160 hours	100%	With load and nominal supply voltage
Final Electrical	Refer to Table I-a, I-b and Detail Specifications			100%	
Percent Defective Allowance (PDA)	38534		Refer to table I-a below		PDA = 2% (Supply Current only)
Seal Fine Leak	883	1014	A1 or B1	100%	(See Note 2)
Seal Gross Leak	883	1014	C, B2 or B3	100%	(See Note 2)
Radiographic Inspection	883	2012	Class S	100%	
Frequency Aging 30 days	55310		+70°C±3°C Refer to Table I-a below	100%	(See Note 1)
External Visual	883	2009		100%	

NOTES:

1. Normally frequency aging is up to 30 days. However, aging may be ceased if value at 15 days is half than the limit of 30-day aging value, or continued up to 90 days if value exeeds 30 day aging limit.
2. Unless otherwise specified, Q-Tech uses conditions A1 and C for Fine and Gross Leak. Fine Leak Rate is $5x10^{-8}$ atm-cm^3/s Helium gas. Condition B3 is used if free internal cavity volume is < 0.1cc.

Table I-a
Delta Limits

Tests	Parameters	Symbol	Delta Limits
Burn-In # 2	Supply current	Icc	±10% of initial reading
Life Test after 1,000 hours at +125°C	Supply current	Icc (Life)	±10% of initial reading
Frequency Aging after 30 days at +70°C	Output Frequency	Fo	Refer to detailed specifications

Screening - Option S (Continued)

Table I-b
Electrical Test - Measurement Requirements

Parameters	Pre BI at 25°C	Pre BI Low Temp	Pre BI High Temp	Interim BI at 25°C	Post BI at 25°C	Post BI Low Temp	Post BI High Temp
Output Frequency	✓	✓	✓	✓	✓	✓	✓
Frequency/Temperature Stability	✓	✓	✓	✓	✓	✓	✓
Frequency/Voltage Stability	✓				✓	✓	✓
Input Current	✓			✓	✓	✓	✓
Output Voltage (VOH, VOL) **(Note 3)**	✓	✓	✓	✓	✓	✓	✓
Waveform	✓	✓	✓	✓	✓	✓	✓
Duty Cycle	✓	✓	✓	✓	✓	✓	✓
Rise and Fall Times	✓			✓	✓	✓	✓
Start-up Time	✓			✓	✓	✓	✓
Tristate Function **(If Applicable)**	✓				✓	✓	✓

NOTES:

1. Frequency Stability code 19, measure frequency parameter at +23ºC ± 1ºC.
2. Frequency accuracy (and/or frequency/temperature stability) limits for post steady state life electrical testing shall be relaxed by six times the projected first year aging limit as specified in this specification. If no such limit is specified, the limit shall be relaxed ±60ppm. Notwithstanding, device performance that appears out-of-family shall be subjected to further evaluation.
3. Differential Output Voltage (VOD) is also tested for LVDS output logic.

Table I-c
Group A Inspection (100%)

Test Description	Condition
Supply Current	25°C and temperature extremes
Initial Accuracy at Reference Temperature	25°C
Frequency - Temperature Stability	Over specified operating temperature range, measure output frequency at minimum ten equispaced points of the temperature extremes.
Frequency - Voltage Tolerance	25°C and temperature extremes
Output Voltages (VOH, VOL) **(Note 2)**	
Duty Cycle (output waveform symmetry)	
Output Rise and Fall Times	
Start-up Time	
Tristate Function **(If Applicable)**	

NOTES:

1. Frequency Stability code 19, measure frequency parameter at +23ºC ± 1ºC.
2. Differential Output Voltage (VOD) is also tested for LVDS output logic.
3. All electrical performance tests shall be performed during Group A with the exception of any tests performed as part of final electrical testing during 100 percent screening.

QCI Options (per MIL-PRF-55310, level S)

- Group C Inspection per MIL-PRF-55310, Level S *(See details on Table X)*

QCI (per MIL-PRF-38534, Class K-Modified) (To be specified on Purchase Order)

- Group B Inspection per MIL-PRF-38534, Class K-Modified *(See details on Table VII)*
- Group C Inspection per MIL-PRF-38534, Class K-Modified (Delta Limits per Table I-a) *(See details on Table VIII)*
- Group D Inspection per MIL-PRF-38534, Class K-Modified *(See details on Table IX)*

Screening Option A (MIL-PRF-55310, Level S)

(Example: QT188ACD10A-40.000MHz)

Table II

Test Description	MIL Standard	Method	Condition	Qty	Comments
Non Destructive Bond Pull	883	2023	Level S	100%	Completed During Assembly
Internal Visual	883	2017 2032	Class K	100%	
Stabilization Bake	883	1008	C 48 hours at +150°C	100%	
Pre-Random Vibration Electrical	Refer to Table II-a and Detail Specification			100%	
Random Vibration	883	2026	I-B	100%	Three mutually perpendicular directions
Post-Random Vibration Electrical	Refer to Table II-a and Detail Specification			100%	
Thermal Shock	883	1011	A	100%	
Temperature Cycling	883	1010	C	100%	10 cycles
Constant Acceleration	883	2001	A	100%	Y1 direction only (5,000g's)
Seal Fine and Gross Leak	883	1014	A1, A2 or B1 B2 or B3	100%	See Note 2
Particle Impact Noise Detection (PIND)	883	2020	A	100%	
Pre Burn-In Electrical	Refer to Table II-a and Detail Specification			100%	
Burn-In	883	1015	+125°C for 240 hours minimum	100%	With load and nominal supply voltage
Final Electrical	Refer to Table II-a and Detail Specification			100%	
Percent Defective Allowance (PDA)	55310		Level S		PDA=2% or 1 unit (Supply Current ± 10%, VOH ± 10% & VOL ± 0.1V at 25ºC only)
Radiographic Inspection	883	2012	Level S	100%	
External Visual	883	2009		100%	

NOTES:

1. 100% QCI Group A (see Table II-b) and Group B (Aging) (see Table II-c) Inspections are performed.
2. Conditions A1 and C are used if B1 and B2 are not purchased. Condition B3 is used if free internal cavity volume is < 0.1cc.

Table II-a
Electrical Test – Measurement Requirements

Parameters	Pre RV at 25ºC	Post RV at 25ºC	Pre BI at 25ºC	Pre BI Low Temp	Pre BI High Temp	Post BI at 25ºC	Post BI Low Temp	Post BI High Temp
Output Frequency	✓	✓	✓	✓	✓	✓	✓	✓
Frequency/Temperature Stability			✓	✓	✓	✓	✓	✓
Frequency/Voltage Stability			✓			✓		
Input current	✓	✓	✓			✓	✓	✓
Output Voltage (VOH, VOL) **(Note 2)**			✓	✓	✓	✓	✓	✓
Waveform			✓	✓	✓	✓	✓	✓
Duty cycle			✓	✓	✓	✓	✓	✓
Rise and Fall Times			✓			✓	✓	✓
Start-up Time			✓			✓	✓	✓
Tristate Function **(If Applicable)**			✓			✓	✓	✓

NOTES:

1. Frequency Stability code 19, measure frequency parameter at +23ºC ± 1ºC.
2. Differential Output Voltage (VOD) is also tested for LVDS output logic.

Screening - Option A (Continued)

Table II-b
Group A Inspection (100%)

Test Description	Condition
Supply Current	25°C and temperature extremes
Initial Accuracy at Reference Temperature	25°C
Frequency - Temperature Stability	Over specified operating temperature range, measure output frequency at minimum ten equispaced points of the temperature extremes.
Frequency - Voltage Tolerance	25°C and temperature extremes
Output Voltages (VOH, VOL) **(Note 2)**	
Duty Cycle (output waveform symmetry)	
Output Rise and Fall Times	
Start-up Time	
Tristate Function **(If Applicable)**	
Overvoltage Survivability	Apply over voltage 20% above maximum specified supply voltage for 1 minute with no performance degradation

NOTES:

1. Frequency Stability code 19, measure frequency parameter at +23ºC ± 1ºC.
2. Differential Output Voltage (VOD) is also tested for LVDS output logic.
3. Subgroup 2 (Solderability) is not required unless otherwise specified on the purchase order.
4. All electrical performance tests shall be performed during Group A with the exception of any tests performed as part of final electrical testing during 100 percent screening.

Table II-c
Group B Inspection (100%)

Test Description	Condition
Frequency Aging	MIL-PRF-55310, Paragraph 4.8.35

NOTES:

1. Frequency aging is up to 30 days. Aging may be ceased if value at 15 days is half than the limit of 30-day aging value.

QCI (per MIL-PRF-55310, Level S) (To be specified on Purchase Order)

- Group C Inspection per MIL-PRF-55310, Level S *(See details on Table X)*

QCI (per MIL-PRF-38534, Class K-Modified) (To be specified on Purchase Order)

- Group B Inspection per MIL-PRF-38534, Class K-Modified *(See details on Table VII)*
- Group C Inspection per MIL-PRF-38534, Class K-Modified (Delta Limits per Table I-a) *(See details on Table VIII)*
- Group D Inspection per MIL-PRF-38534, Class K-Modified *(See details on Table IX)*

Screening Option C (Modified MIL-PRF-55310, Level S)

(Example: QT188LD10C-40.000MHz)

Table III

Test Description	MIL Standard	Method	Condition	Qty	Comments
Non Destructive Bond Pull	883	2023	Level S	100%	Completed During Assembly
Internal Visual	883	2017 2032	Class K	100%	
Stabilization Bake	883	1008	C 48 hours at +150°C	100%	
Pre-Random Vibration Electrical	Refer to Table III-a and Detail Specification			100%	
Random Vibration	883	2026	I-B	100%	Three mutually perpendicular directions
Post-Random Vibration Electrical	Refer to Table III-a and Detail Specification			100%	
Thermal Shock	883	1011	A	100%	
Temperature Cycling	883	1010	C	100%	10 cycles
Constant Acceleration	883	2001	A	100%	Y1 direction only (5,000g's)
Seal Fine and Gross Leak	883	1014	A1, A2 or B1 B2 or B3	100%	See Note 2
Particle Impact Noise Detection (PIND)	883	2020	A	100%	
Pre Burn-In Electrical	Refer to Table III-a and Detail Specification			100%	
Burn-In	883	1015	+125°C for 240 hours minimum	100%	With load and nominal supply voltage
Final Electrical	Refer to Table III-a and Detail Specification			100%	
Percent Defective Allowance (PDA)	55310		Level S		PDA=2% or 1 unit (Supply Current ± 10%, VOH ± 10% & VOL ± 0.1V at 25ºC only)
External Visual	883	2009		100%	

NOTES:

1. 100% QCI Group A Inspection is performed. See Table III-b
2. Conditions A1 and C are used if B1 and B2 are not purchased. Condition B3 is used if free internal cavity volume is < 0.1cc.

Table III-a
Electrical Test – Measurement Requirements

Parameters	Pre RV at 25ºC	Post RV at 25ºC	Pre BI at 25ºC	Pre BI Low Temp	Pre BI High Temp	Post BI at 25ºC	Post BI Low Temp	Post BI High Temp
Output Frequency	✓	✓	✓	✓	✓	✓	✓	✓
Frequency/Temperature Stability			✓	✓	✓	✓	✓	✓
Frequency/Voltage Stability			✓			✓		
Input current	✓	✓	✓			✓	✓	✓
Output Voltage (VOH, VOL) **(Note 2)**			✓	✓	✓	✓	✓	✓
Waveform			✓	✓	✓	✓	✓	✓
Duty cycle			✓	✓	✓	✓	✓	✓
Rise and Fall Times			✓			✓	✓	✓
Start-up Time			✓			✓	✓	✓
Tristate Function **(If Applicable)**			✓			✓	✓	✓

NOTES:

1. Frequency Stability code 19, measure frequency parameter at +23ºC ± 1ºC.
2. Differential Output Voltage (VOD) is also tested for LVDS output logic.

Screening - Option C (Continued)

Table III-b
Group A Inspection (100%)

Test Description	Condition
Supply Current	25°C and temperature extremes
Initial Accuracy at Reference Temperature	25°C
Frequency - Temperature Stability	Over specified operating temperature range, measure output frequency at minimum ten equispaced points of the temperature extremes.
Frequency - Voltage Tolerance	25°C and temperature extremes
Output Voltages (VOH, VOL) **(Note 2)**	
Duty Cycle (output waveform symmetry)	
Output Rise and Fall Times	
Start-up Time	
Tristate Function **(If Applicable)**	

NOTES:

1. Frequency Stability code 19, measure frequency parameter at +23ºC ± 1ºC.
2. Differential Output Voltage (VOD) is also tested for LVDS output logic.
3. All electrical performance tests shall be performed during Group A with the exception of any tests performed as part of final electrical testing during 100 percent screening.

QCI (per MIL-PRF-55310, Level S) (To be specified on Purchase Order)

- Group C Inspection per MIL-PRF-55310, Level S *(See details on Table X)*

QCI (per MIL-PRF-38534, Class K-Modified) (To be specified on Purchase Order)

- Group B Inspection per MIL-PRF-38534, Class K-Modified *(See details on Table VII)*
- Group C Inspection per MIL-PRF-38534, Class K-Modified (Delta Limits per Table I-a) *(See details on Table VIII)*
- Group D Inspection per MIL-PRF-38534, Class K-Modified *(See details on Table IX)*

Screening Option N (EEE-INST-002)

(Example: QT188ND10N-40.000MHz)

Table IV

Test Description	MIL Standard	Method	Condition	Qty	Comments
Non Destructive Bond Pull	883	2023		100%	Completed During Assembly
Internal Visual	883	2017 2032	Class K	100%	
Stabilization Bake	883	1008	C 48 hours at +150°C	100%	
Thermal Shock	883	1011	A	100%	
Temperature Cycling	883	1010	B	100%	10 cycles
Constant Acceleration	883	2001	A	100%	Y1 direction only (5,000g's)
Particle Impact Noise Detection (PIND)	883	2020	B	100%	
Pre Burn-In Electrical	Refer to Table IV-a and Detail Specification			100%	
Burn-In	883	1015	+125°C for 240 hours minimum	100%	With load and nominal supply voltage
Final Electrical	Refer to Table IV-a and Detail Specification			100%	
Frequency Aging	55310		70°C± 3°C	100%	30 Days
Percent Defective Allowance (PDA)	55310		Level S		PDA=5% (Supply Current only Frequency Aging)
Radiographic Inspection	883	2012	Class S	100%	
Seal Fine and Gross Leak	883	1014	A1 or B1 C	100%	See Note 2
External Visual	883	2009		100%	

NOTES:

1. 100% QCI Group A Inspections are performed. See Table IV-b
2. Unless otherwise specificed, Q-Tech uses conditions A1 and C for Fine and Gross Leak. Fine Leak Rate is $5x10^{-8}$ atm-cm^3/s Helium gas. Condition B3 is used if free internal cavity volume is < 0.1cc.

Table IV-a
Electrical Test – Measurement Requirements

Parameters	Pre BI at 25°C	Pre BI Low Temp	Pre BI High Temp	Post BI at 25°C	Post BI Low Temp	Post BI High Temp
Output Frequency	✓	✓	✓	✓	✓	✓
Frequency/Temperature Stability	✓	✓	✓	✓	✓	✓
Frequency/Voltage Stability	✓			✓		
Input current	✓			✓	✓	✓
Output Voltage (VOH, VOL) **(Note 2)**	✓	✓	✓	✓	✓	✓
Waveform	✓	✓	✓	✓	✓	✓
Duty cycle	✓	✓	✓	✓	✓	✓
Rise and Fall Times	✓			✓	✓	✓
Start-up Time	✓			✓	✓	✓
Tristate Function **(If Applicable)**	✓			✓	✓	✓

NOTES:

1. Frequency Stability code 19, measure frequency parameter at +23ºC ± 1ºC.
2. Differential Output Voltage (VOD) is also tested for LVDS output logic.

Screening - Option N (Continued)

Table IV-b
Group A Inspection (100%)

Test Description	Condition
Supply Current	25°C and temperature extremes
Initial Accuracy at Reference Temperature	25°C
Frequency - Temperature Stability	Over specified operating temperature range, measure output frequency at minimum ten equispaced points of the temperature extremes.
Frequency - Voltage Tolerance	25°C and temperature extremes
Output Voltages (VOH, VOL) **(Note 2)**	
Duty Cycle (output waveform symmetry)	
Output Rise and Fall Times	
Start-up Time	
Tristate Function **(If Applicable)**	
Oscillator Supply Voltage	Measure voltage magnitude, tolerance, polarity, regulation, peak to peak ripple, ripple frequency and noise across oscillator input terminals with specified load
Overvoltage Survivability	Apply over voltage 20% above maximum specified supply voltage for 1 minute with no performance degradation

NOTES:
1. Frequency Stability code 19, measure frequency parameter at +23ºC ± 1ºC.
2. Differential Output Voltage (VOD) is also tested for LVDS output logic.

Table IV-c
Qualification Test Requirements (Note 1)

Test Description	Test Methods and Conditions	Quantity
GROUP 1 Frequency Aging	MIL-PRF-55310, par. 4.8.35	8(0)
GROUP 2 (Note 3) Vibration Sine Mechanical Shock	MIL-STD 202, Method 204 and MIL-PRF-55310, par. 4.8.39.1 MIL-STD-202, Method 213 and MIL-PRF-55310, par 4.8.41	8(0)
GROUP 3 (Note 3) Thermal Shock	MIL-STD-202, Method 107 and MIL-PRF-55310, par. 4.8.45	4(0)
GROUP 4 (Note 3) Resistance to Soldering Heat Moisture Resistance Terminal Strength Solderability Resistance to Solvents	MIL-STD 202, Method 210 and MIL-PRF-55310, par. 4.8.49 MIL-STD 202, Method 106 and MIL-PRF-55310, par. 4.8.50 MIL-STD 202, Method 211 and MIL-PRF-55310, par 4.8.52 MIL-STD 202, Method 208, each lead MIL-STD 202, Method 215	2(0)
GROUP 5 (Note 5, 6) Internal Gas Analysis	MIL-STD 883, Method 1018, 5000ppm at 100°C	3(0) or 5(1)

NOTES: 1) Performed only if specified on the Purchase Order.
2) Sample units shall have previously met all requirements of the previous test of Table IV-a.
3) Samples for this group come from Group 1 samples
4) Generic data less than 1 year old is an acceptable basis for qualification if it satisfies the requirements specified herein.
5) Applies only to hybrid microcircuit construction. Generic data is not acceptable.
6) Units tested in Group 5 shall be independent units not tested in Groups 1 - 4.

Screening - Option B (Modified MIL-PRF-55310, Level B)

(Example: QT178LD10B-50.000MHz)

Table V

Test Description	MIL Standard	Method	Condition	Qty	Comments
Internal Visual	883	2017	Level B	100%	Completed During Assembly
Stabilization Bake	883	1008	C 48 hours at +150°C	100%	
Temperature Cycling	883	1010	B	100%	10 cycles
Constant Acceleration	883	2001	A	100%	Y1 direction only (5,000g's)
Particle Impact Noise Detection (PIND)	883	2020	B	100%	
Pre Burn-In Electrical	Refer to Table V-a and Detail Specification			100%	
Burn-In	883	1015	+125°C for 160 hours	100%	With load and nominal supply voltage
Final Electrical	Refer to Table V-a and Detail Specification			100%	
Percent Defective Allowance (PDA)	38534				PDA=10% (Supply Current only)
Seal Fine Leak	883	1014	A1	100%	
Seal Gross Leak	883	1014	C	100%	
External Visual	883	2009		100%	

NOTES:

1. 100% Group A QCI test per Table V-b.

Table V-a
Electrical Test - Measurement Requirements

Parameters	Pre BI at 25°C	Pre BI Low Temp	Pre BI High Temp	Post BI at 25°C	Post BI Low Temp	Post BI High Temp
Output Frequency	✓	✓	✓	✓	✓	✓
Frequency/Temperature Stability	✓	✓	✓	✓	✓	✓
Frequency/Voltage Stability	✓			✓		
Input current	✓			✓	✓	✓
Output Voltage (VOH, VOL) **(Note 2)**	✓	✓	✓	✓	✓	✓
Waveform	✓	✓	✓	✓	✓	✓
Duty cycle	✓	✓	✓	✓	✓	✓
Rise and Fall Times	✓			✓	✓	✓
Start-up Time	✓			✓	✓	✓
Tristate Function **(If Applicable)**	✓			✓	✓	✓

NOTES:

1. Frequency Stability code 19, measure frequency parameter at +23°C ± 1°C.
2. Differential Output Voltage (VOD) is also tested for LVDS output logic.

Screening - Option B (Continued)

Table V-b
Group A Inspection (100%)

Test Description	Condition
Supply Current	25°C and temperature extremes
Initial Accuracy at Reference Temperature	25°C and temperature extremes
Frequency - Temperature Stability	Over specified operating temperature range, measure output frequency at minimum ten equispaced points of the temperature extremes.
Frequency - Voltage Tolerance	25°C and temperature extremes
Output Voltages (VOH, VOL) **(Note 2)**	
Duty Cycle (output waveform symmetry)	
Output Rise and Fall Times	
Start-up Time	
Tristate Function	

NOTES:

1. Frequency Stability code 19, measure frequency parameter at +23ºC ± 1ºC.
2. Differential Output Voltage (VOD) is also tested for LVDS output logic.
3. All electrical performance tests shall be performed during Group A with the exception of any tests performed as part of final electrical testing during 100 percent screening.

QCI (per MIL-PRF-55310, Level B) (To be specified on Purchase Order)

- Group B (Aging Test)
- Group C *(See details on Table X).*

QCI Options (per MIL-PRF-38534, Class K-Modified)

- Group B Inspection per MIL-PRF-38534, Class K-Modified *(See details on Table VII)*
- Group C Inspection per MIL-PRF-38534, Class K-Modified (Delta Limits per Table II) *(See details on Table VIII)*
- Group D Inspection per MIL-PRF-38534, Class K-Modified *(See details on Table IX)*

Screening Option E (Engineering Model)

(Example: QT122ACD9E-16.000MHz)

Table VI

Test Description	MIL Standard	Method	Condition	Qty	Comments
Internal Visual	883	2017	Class H	100%	Completed During Assembly
Stabilization Bake	883	1008	C 48 hours at +150°C	100%	
Seal Fine and Gross Leak	883	1014	A1, C	100%	
Final Electrical	Refer to Table VI-a and Detail Specification			100%	
Frequency vs. Temperature Stability	55310	Measure output frequency at 10 equispaced points minimum of the specified operating temperature range		100%	
External Visual	883	2009		100%	

Table VI-a
Electrical Test – Measurement Requirements

Parameters	Final at 25°C	Final Low Temp	Final High Temp
Output Frequency	✓	✓	✓
Frequency/Temperature Stability	✓	✓	✓
Frequency/Voltage Stability	✓	✓	✓
Input Current	✓		
Output Voltage (VOH, VOL) **(Note 2)**	✓		
Waveform	✓		
Duty Cycle	✓		
Rise and Fall Times	✓		
Start-up Time	✓		
Tristate Function **(If Applicable)**	✓		

NOTES:

1. Frequency Stability code 19, measure frequency parameter at +23ºC ± 1ºC.
2. Differential Output Voltage (VOD) is also tested for LVDS output logic.

Engineering model oscillators will have the same design and manufacturing processes as to the flight units. Finished units will be tested over the operating temperature range and 25ºC as specified in Table VI-a. No screening test and/or QCI are required.

Electrical Performance Characteristics 15kHz to 85MHz

(For FACT +5Vdc and +3.3Vdc CMOS Outputs Using 54ACT3301)

Maximum Ratings

Parameters	Symbol	Min.	Max.	Units
Supply Voltage	Vdd	-0.5	+7	V
Operating Temperature	Top.	-55	+125	°C
Storage Temperature	Tstg	-62	+125	°C
Lead Solder Temperature			260/10	°C/seconds
Package Thermal Resistance	ΘJc		50	°C/W
Junction Temperature			+175	ºC

Recommended Operating Conditions

Electrical Parameter	Test Conditions	Limits				Notes
		Min.	Nom.	Max.	Units	
Frequency Range	+3.3Vdc	.015 .450		80 70	MHz MHz	DIP, Flat Packs Other Packages
	+5.0Vdc	.015 .450		85 85	MHz MHz	DIP, Flat Packs Other Packages
Frequency/Temperature Stability	See temperature codes	-55	+25	+125	°C	(See Note 1)
Supply Voltage		2.97 4.5	3.3 5.0	3.63 5.5	Vdc Vdc	
Input Current at 3.63Vdc	Measured without load at maximum Vdd			3 6 10 20 30	mA	15k ≤ F < 500kHz 500k ≤ F < 16MHz 16M ≤ F < 32MHz 32M ≤ F < 60MHz 60M ≤ F ≤ 80MHz
Input Current at 5.5Vdc	Measured without load at maximum Vdd			20 25 35 45	mA	15k-<16MHz 16M-<32MHz 32M-<60MHz 60M-85MHz
Output Voltage VOL				Vdd x 0.1 0.4 (TTL)	Vdc	(See Note 4)
Output Voltage VOH		Vdd x 0.9 2.4 (TTL)			Vdc	(See Note 4)
Output Waveform		Square Wave			N/A	
Rise and Fall Time (See Note 4)	See Notes 5 and 6			6	ns	15k ≤ F < 30MHz 5x7mm: 450kHz ≤ F ≤ 44MHz
	See Notes 5 and 6			3	ns	30M ≤ F < 85MHz 5x7mm: 44M < F ≤ 85MHz
Duty Cycle (See Note 4)	See Notes 5 and 6	45 40	50 50	55 60	% %	15k ≤ F <16MHz 16M ≤ F ≤ 85MHz
Load		15pF//10kΩ (CMOS) 6TTL to 10TTL (TTL)				Per MIL-PRF-55310 loads (See Note 4)
Frequency Aging - 30 Days (See Note 2)	70°C±3°C			±1.5	ppm	
	70°C±3°C			±3	ppm	5x7 packages only
Frequency Aging, First Year	70°C±3°C			±5	ppm	(See Note 3)
Frequency Aging, First Year (5x7 Packages)	70°C±3°C			±10	ppm	(See Note 3)
Start-up Time	100µs ramp			10	ms	
Output Enable VIH		2.2			Vdc	
Output Disable VIL				0.8	Vdc	Output High Impedance
Frequency Voltage Tolerance	over ±10% change in supply voltage	-3		+3	ppm	DIP, FP at 5V: 15kHz ≤ F ≤ 27MHz 36MHz ≤ F ≤ 85MHz
		-4		+4		DIP, FP at 3.3V and Ceramic, TO pkgs: 15kHz ≤ F ≤ 27MHz, 36MHz ≤ F ≤ 85MHz
		-5		+5		27MHz < F < 36MHz

NOTES:

1. Frequency stability compared to nominal frequency including initial accuracy at 25°C, load, and supply variations ±10%. Frequency Stability code 19, measure frequency parameter at +23ºC ± 1ºC.
2. Normally frequency aging is up 30 days. However, aging may be ceased if value at 15 days is half than the limit of 30-day aging value, or continued up to 90 days if value exeeds 30 day aging limit for screening options "S".
3. Aging is ±5/±10ppm after first year and ±2ppm/year thereafter.
4. AC logic (+5Vdc) is HCMOS & TTL compatible.
5. For CMOS, Duty Cycle is measured at 50% of Output and Rise and Fall Time is measured between 10% and 90% of the waveform.
6. For TTL, Duty Cycle is measured at 1.4Vdc and Rise and Fall Time is measured between 0.8V and 2.0V.

Electrical Performance Characteristics 40MHz to 200MHz CMOS

(For BiCMOS +1.8Vdc, +2.5Vdc, +3.3Vdc CMOS Ouputs)

Maximum Ratings

Parameters	Symbol	Min.	Max.	Units
Supply Voltage	Vdd	-0.5	+5	V
Operating Temperature	Top.	-55	+125	°C
Storage Temperature	Tstg	-62	+125	°C
Lead Solder Temperature			260/10	°C/seconds
Package Thermal Resistance	ΘJc		50	°C/W
Junction Temperature			+150	ºC

Recommended Operating Conditions

Electrical Parameter	Test Conditions	Limits				Notes
		Min.	Nom.	Max.	Units	
Frequency Range	+1.8Vdc	40		100	MHz	All Packages
	+2.5Vdc	40		133		DIP, Flat Packs
		70		133		All Other Packages
	+3.3Vdc	70		200		DIP, Flat Packs
		70		184.32		All Other Packages
Frequency/Temperature Stability	See temperature codes	-55	+25	+125	°C	(See Note 1)
Supply Voltage	+1.8Vdc	1.62	1.8	1.98	Vdc	
	+2.5Vdc	2.25	2.5	2.75		
	+3.3Vdc	2.97	3.3	3.63		
Input Current (Option L - 3.3Vdc)	Measured without load at maximum Vdd			30 40 50	mA	40M ≤ F < 100MHz 100M ≤ F < 130MHz 130M ≤ F ≤ 200MHz
Input Current (Option N - 2.5Vdc)	Measured without load at maximum Vdd			15 25 35	mA	40M ≤ F <60MHz 60M ≤ F <85MHz 85M ≤ F ≤ 133MHz
Input Current (Option R - 1.8Vdc)	Measured without load at maximum Vdd			10 20 25	mA	40M ≤ F < 50MHz 50M ≤ F < 85MHz 85M ≤ F ≤ 100MHz
Output Voltage VOL				Vdd x 0.1	Vdc	
Output Voltage VOH		Vdd x 0.9			Vdc	
Output Waveform		Square Wave			N/A	
Rise and Fall Time	10% to 90%			3	ns	
Duty Cycle	50% of output	40		60	%	
Load		15pF//10kΩ				
Frequency Aging - 30 days (See Note 2)	70°C±3°C			±1.5 ±2 ±3 ±4	ppm ppm ppm ppm	40M - 150MHz >150M - 200MHz 40 - 85MHz (5x7 packages only) F > 85MHz (5x7 packages only)
Frequency Aging, First Year	70°C±3°C			±5	ppm	(See Note 3)
	70°C±3°C			±10	ppm	5x7 packages only (See Note 3)
Start-up Time	100µs ramp			10	ms	
Output Enable VIH		0.7 x Vdd			Vdc	
Output Disable VIL				0.3 x Vdd	Vdc	Output High Impedance
Frequency Voltage Tolerance	Over ±10% change in supply voltage	-3		+3	ppm	DIP, FP: 40MHz ≤ F ≤ 165MHz
		-4		+4		All Ceramic Packages: 40MHz ≤ F ≤ 165MHz
		-5		+5		All Packages F > 165MHz

NOTES:

1. Frequency stability compared to nominal frequency including initial accuracy at 25°C, load, and supply variations ±10%. Frequency Stability code 19, measure frequency parameter at +23ºC ± 1ºC.
2. Normally frequency aging is up 30 days. However, aging may be ceased if value at 15 days is half than the limit of 30-day aging value, or continued up to 90 days if value exeeds 30 day aging limit for screening option "S".
3. Aging is ±5/±10ppm after first year and ±2ppm/year thereafter.
4. Please see Paragraph 3.5.4.1 (page 3) for Scanning Electron Microscopy (SEM) on potential metallization thinning on the active die used in these designs - VC5035AL, Class K.

Electrical Performance Characteristics 450kHz to 40MHz CMOS

(For CMOS +1.8Vdc and +2.5Vdc CMOS Ouputs)

Maximum Ratings

Parameters	Symbol	Min.	Max.	Units
Supply Voltage	Vdd	-0.5	+5	V
Operating Temperature	Top.	-55	+125	°C
Storage Temperature	Tstg	-62	+125	°C
Lead Solder Temperature			260/10	°C/seconds
Package Thermal Resistance	ΘJc		50	°C/W
Junction Temperature			+150	ºC

Recommended Operating Conditions

Electrical Parameter	Test Conditions	Limits				Notes
		Min.	Nom.	Max.	Units	
Frequency Range	+1.8Vdc	0.450		40	MHz	All Packages
	+2.5Vdc	0.450		40	MHz	All Packages
Frequency/Temperature Stability	See temperature codes	-55	+25	+125	°C	(See Note 1)
Supply Voltage	+1.8Vdc	1.62	1.8	1.98	Vdc	
	+2.5Vdc	2.25	2.5	2.75	Vdc	
Input Current (Option R - 1.8Vdc)	Measured without load at maximum Vdd			4	mA	450kHz - 40MHz
Input Current (Option N - 2.5Vdc)				3 6	mA	450kHz - <500kHz 500kHz - 40MHz
Output Voltage VOL				Vdd x 0.1	Vdc	
Output Voltage VOH		Vdd x 0.9			Vdc	
Output Waveform		Square Wave			N/A	
Rise and Fall Time	10% to 90%			6 4	ns	450kHz - <20MHz 20MHz - 40MHz
Duty Cycle	50% of output	45 40		55 60	%	450kHz - <15MHz 15MHz - 40MHz
Load		15pF//10kΩ				
Frequency Aging after 30 days	70°C±3°C			±1.5	ppm	(See Note 2)
Frequency Aging, First Year	70°C±3°C			±5	ppm	(See Note 3)
Start-up Time	100µs ramp			10	ms	
Output Enable VIH		0.7 x Vdd			Vdc	
Output Disable VIL				0.3 x Vdd	Vdc	Output High Impedance
Frequency Voltage Tolerance	Over ±10% change in supply voltage	-4		+4	ppm	All Packages

NOTES:

1. Frequency stability compared to nominal frequency including initial accuracy at 25°C, load, and supply variations ±10%. Frequency Stability code 19, measure frequency parameter at +23ºC ± 1ºC.
2. Normally frequency aging is up 30 days. However, aging may be ceased if value at 15 days is half than the limit of 30-day aging value, or continued up to 90 days if value exeeds 30 day aging limit for screening option “S”.
3. Aging is ±5ppm after first year and ±2ppm/year thereafter.

Electrical Performance Characteristics 40MHz to 250MHz LVDS

(For BiCMOS +2.5Vdc and +3.3Vdc LVDS Ouputs)

Maximum Ratings

Parameters	Symbol	Min.	Max.	Units
Supply Voltage	Vdd	-0.5	+5	V
Operating Temperature	Top.	-55	+125	°C
Storage Temperature	Tstg	-62	+125	°C
Lead Solder Temperature			260/10	°C/seconds
Package Thermal Resistance	ΘJc		50	°C/W
Junction Temperature			+150	ºC

Recommended Operating Conditions

Electrical Parameter	Test Conditions	Limits				Notes
		Min.	Nom.	Max.	Units	
Frequency Range	+2.5Vdc	80		250	MHz	Flat Packs, QT93, QT94
		80		162.5		5x7mm Packages
	+3.3Vdc	40		250		Flat Packs, QT93, QT94
		40		162.5		5x7mm Packages
Frequency/Temperature Stability	See temperature codes	-55	+25	+125	°C	(See Note 1)
Supply Voltage		3.135 2.375	3.3 2.5	3.465 2.625	Vdc Vdc	
Input Current	Measured without load at maximum Vdd			66 80	mA mA	F > 250MHz
Output Voltage VOL		0.90	1.1		Vdc	
Output Voltage VOH			1.45	1.65	Vdc	
Differential Output Voltage (VOD)		247	330	454	mV	
Offset Voltage (VOS)		1.125	1.25	1.375	V	
Output Waveform		Square Wave			N/A	
Rise and Fall Time	20% to 80%			1000 600	ps	40MHz ≤ F < 80MHz F ≥ 80MHz
Duty Cycle	50% of output	45	50	55	%	
Load		100Ω (Connected between Q+ & Q-)			Ω	
Frequency Aging after 30 days (See Note 2)	70°C±3°C			±1.5 ±2 ±3 ±3.5 ±3 ±4	ppm ppm ppm ppm ppm ppm	40MHz < F < 150MHz 150MHz < F < 200MHz 200MHz < F < 250MHz F > 250MHz 40 - 80MHz (5x7 packages only) F > 80MHz (5x7 packages only)
Frequency Aging, First Year	70°C±3°C			±5 ±10	ppm	F < 150MHz F ≥ 150MHz (See Note 3)
Frequency Aging, First Year (5x7 packages)	70°C±3°C			±10 ±15	ppm	F ≤ 80MHz F > 80MHz (See Note 3)
Start-up Time	100µs ramp			10	ms	
Output Enable VIH		0.7xVcc			Vdc	
Output Disable VIL				0.3xVcc	Vdc	Output High Impedance
Frequency Voltage Tolerance	Over Vcc ± 5%	-4		+4	ppm	All Packages

NOTES:

1. Frequency stability compared to nominal frequency including initial accuracy at 25°C, load, and supply variations ±5%. Frequency Stability code 19, measure frequency parameter at +23ºC ± 1ºC.
2. Normally frequency aging is up 30 days. However, aging may be ceased if value at 15 days is half than the limit of 30-day aging value, or continued up to 90 days if value exeeds 30 day aging limit.
3. Aging is ±5/±10/±15ppm after first year and ±2ppm/year thereafter.
4. Please see Paragraph 3.5.4.1 (page 3) for Scanning Electron Microscopy (SEM) on potential metallization thinning on the active die used in these designs - VC5037, Class K.

Electrical Performance Characteristics 80MHz to 250MHz LVPECL

(For BiCMOS +2.5Vdc and +3.3Vdc LVPECL Ouputs)

Maximum Ratings

Parameters	Symbol	Min.	Max.	Units
Supply Voltage	Vdd	-0.5	+5	V
Operating Temperature	Top.	-55	+125	°C
Storage Temperature	Tstg	-62	+125	°C
Lead Solder Temperature			260/10	°C/seconds
Package Thermal Resistance	ΘJc		50	°C/W
Junction Temperature			+150	°C

Recommended Operating Conditions

Electrical Parameter	Test Conditions	Limits				Notes
		Min.	Nom.	Max.	Units	
Frequency Range	+2.5Vdc	80		200	MHz	Flat Packs, QT193, QT194
		80		162.5		5x7mm Packages
	+3.3Vdc	80		250		Flat Packs, QT193, QT194
		80		162.5		5x7mm Packages
Frequency/Temperature Stability	See temperature codes	-55	+25	+125	°C	(See Note 1)
Supply Voltage		3.135 2.375	3.3 2.5	3.465 2.625	Vdc Vdc	
Input Current	Measured without load at maximum Vdd		60	88	mA	
Output Voltage VOL	3.3V	1.470	1.600	1.745	Vdc	
	2.5V	1.415	1.495	1.620	Vdc	
Output Voltage VOH	3.3V	2.215	2.295	2.420	Vdc	
	2.5V	0.670	0.800	1.195	Vdc	
Output Waveform		Square Wave			N/A	
Rise and Fall Time	20% to 80%		300	700	ps	
Duty Cycle	50% of output	45	50	55	%	
Load		50Ω to Vcc-2V			Ω	or Thevenin equivalent
Output Swing Vopp	3.3V	0.4			V	peak to peak of single output waveform
	2.5V	0.2			V	peak to peak of single output waveform
Frequency Aging after 30 days (See Note 2)	70°C±3°C			±1.5 ±2 ±3 ±3 ±4	ppm ppm ppm ppm ppm	80M < F < 150MHz 150M < F < 200MHz 200M ≤ F ≤ 250MHz 40M ≤ F ≤ 80MHz (5x7 packages only) F > 80MHz (5x7 packages only)
Frequency Aging, First Year	70°C±3°C			±5 ±10	ppm	F < 150MHz F ≥ 150MHz (See Note 3)
Frequency Aging, First Year (5x7 packages)	70°C±3°C			±10 ±15	ppm	F ≤ 80MHz F > 80MHz (See Note 3)
Start-up Time	100µs ramp			10	ms	
Output Enable VIH		0.7xVcc			Vdc	
Output Disable VIL				0.3xVcc	Vdc	Output High Impedance
Frequency Voltage Tolerance	Over Vcc ± 5%	-4		+4	ppm	All Packages

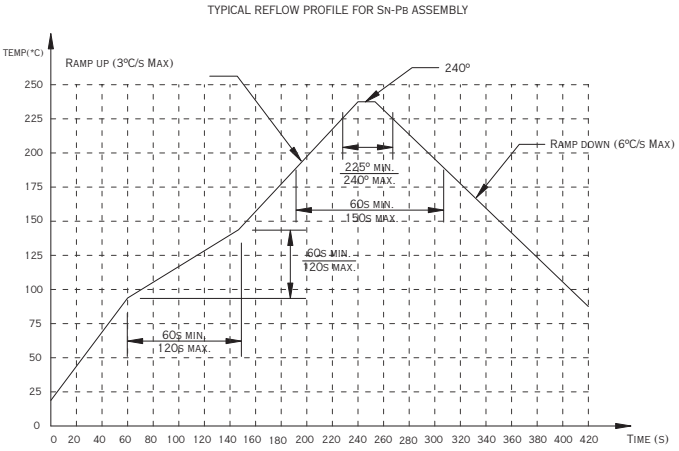
NOTES

1. Frequency stability compared to nominal frequency including initial accuracy at 25°C, load, and supply variations ±5%. Frequency Stability code 19, measure frequency parameter at +23ºC ± 1ºC.
2. Normally frequency aging is up 30 days. However, aging may be ceased if value at 15 days is half than the limit of 30-day aging value, or continued up to 90 days if value exeeds 30 day aging limit for screening options “S” only.
3. Aging is ±5/±10/±15ppm after first year and ±2ppm/year thereafter.
4. Please see Paragraph 3.5.4.1 (page 3) for Scanning Electron Microscopy (SEM) on potential metallization thinning on the active die used in these designs - VC5036, Class K.

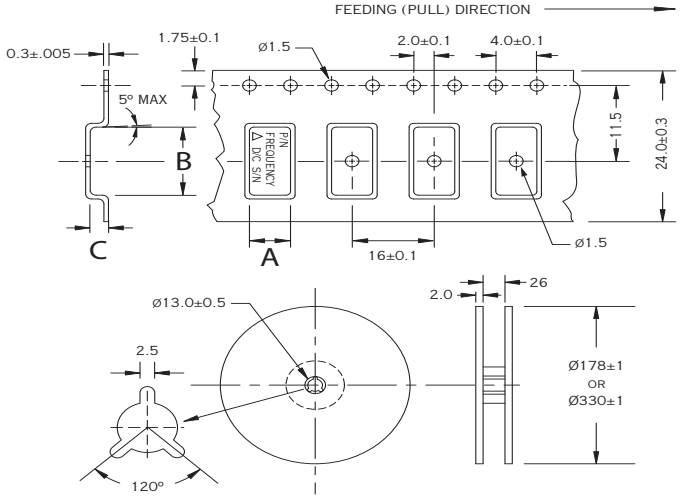
Reflow Profile

The five transition periods for the typical reflow process are:

- Preheat
- Flux activation
- Thermal equalization
- Reflow
- Cool down



Embossed Tape and Reel Information



Dimensions are in mm. Tape is compliant to EIA-481-A.

QT	A	B	C
QT178	10.01 ±0.1	14.53 ±0.1	4.80 ±0.1
QT182	5.72 ±0.1	7.70 ±0.1	4.10 ±0.1
QT183	7.65 ±0.1	9.50 ±0.1	4.70 ±0.1
QT184	5.35 ±0.1	7.75 ±0.1	1.85 ±0.1
QT190	9.470 ±0.1	11.92 ±0.1	6.16 ±0.1
QT188, 192, 193	8.71 ±0.1	9.55 ±0.1	5.34 ±0.1

Reel size vs. quantity:

Reel size (Diameter in mm)	Qty per reel (pcs)		
	QT178	QT184	QT183,188,190,192,193
178	250	1000	150
330	1000		800

Environmental Specifications

Q-Tech Standard Screening/QCI (MIL-PRF-38534 or MIL-PRF-55310) is available for all of our B+ Products. Q-Tech can also customize screening and test procedures to meet your specific requirements. The B+ product is designed and processed to exceed the following test conditions:

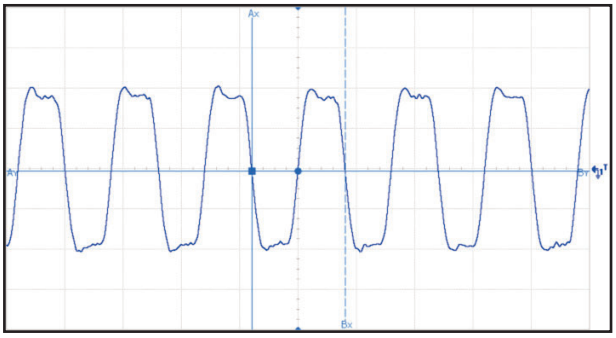
Environmental Test	Test Conditions
Temperature Cycling	MIL-STD-883, Method 1010, Cond. B or Cond. C
Constant Acceleration	MIL-STD-883, Method 2001, Cond. A, Y1
Seal: Fine and Gross Leak	MIL-STD-883, Method 1014, Cond. A, B1 and B2, B3, C
Burn-in	160 hours, 240 hours, or 2 at 160 hours, 125°C with load
Aging	30 days, 70°C, ±1.5ppm max
Vibration, Sinusoidal	MIL-STD-202, Method 204
Random Vibration	MIL-STD-883, Method 2026
Shock, Non-operating	MIL-STD-202, Method 213, Cond. I (See Note 1)
Thermal Shock, Non-operating	MIL-STD-202, Method 107, Cond. B
Ambient Pressure, Non-operating	MIL-STD-202, 105, Cond. C, 5 minutes dwell time minimum
Resistance to Soldering Heat	MIL-STD-202, Method 210
Moisture Resistance	MIL-STD-202, Method 106
Terminal Strength / Lead Integrity	MIL-STD-202, Method 211 / MIL-STD-883, Method 2004 or 2028
Resistance to Solvents	MIL-STD-202, Method 215
Solderability	MIL-STD-202, Method 208
ESD Classification	MIL-STD-883, Method 3015, Class 1C HBM (1000 to 1999 Volts)
Moisture Sensitivity Level	J-STD-020, MSL=1

Note 1: Additional shock results successfully passed on 16MHz, 40MHz, and 80MHz

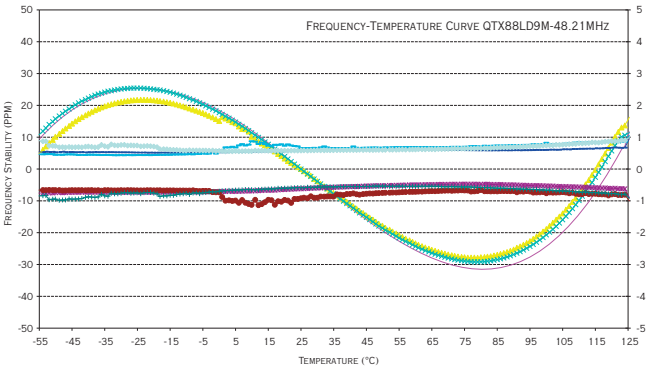
- Shock 850g peak, half-sine, 1 ms duration (MIL-STD-202, Method 213, Cond. D modified)
- Shock 1,500g peak, half-sine, 0.5ms duration (MIL-STD-883, Method 2002, Cond. B)
- Shock 36,000g peak, half-sine, 0.12 ms duration (QT188, QT190 & QT192, QT193, QT194)

Please contact Q-Tech for higher shock requirements

Differential Output of a QT393NW10M-312.500MHz



Frequency vs. Temperature Curve



Thermal Characteristics

The heat transfer model in a hybrid package is described in figure 1.

Heat spreading occurs when heat flows into a material layer of increased cross-sectional area. It is adequate to assume that spreading occurs at a 45° angle.

The total thermal resistance is calculated by summing the thermal resistances of each material in the thermal path between the device and hybrid case.

$$RT = R1 + R2 + R3 + R4 + R5$$

The total thermal resistance RT (see figure 2) between the heat source (die) to the hybrid case is the Theta Junction to Case (Theta JC) in°C/W.

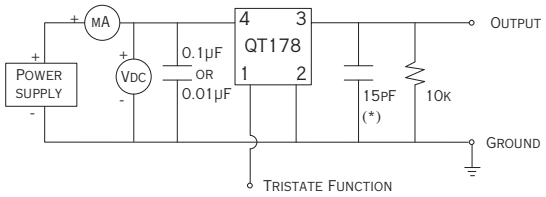
- Theta junction to case (Theta JC) for this product is 30°C/W.
- Theta case to ambient (Theta CA) for this part is 100°C/W.
- Theta Junction to ambient (Theta JA) is 130°C/W.

Maximum power dissipation PD for this package at 25°C is:

- PD(max) = (TJ (max) – TA)/Theta JA
- With TJ = 175°C (Maximum junction temperature of die)
- PD(max) = (175 – 25)/130 = 1.15W

Test Circuit

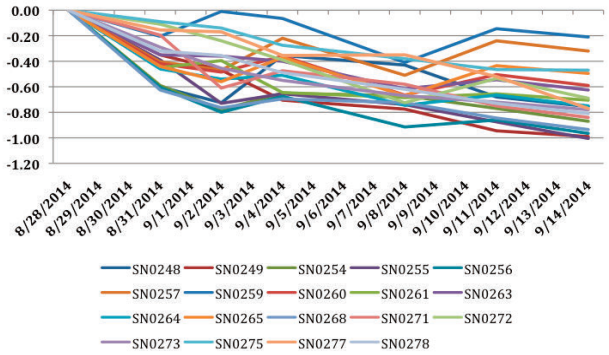
TYPICAL TEST CIRCUIT FOR CMOS LOGIC

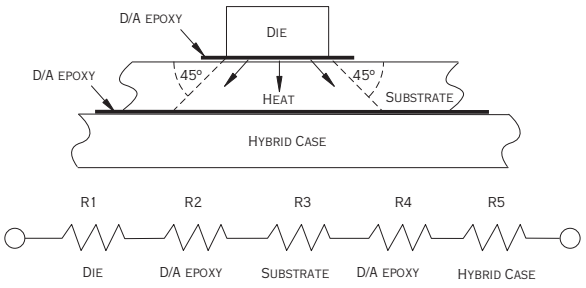


(*) CL INCLUDES PROBE AND JIG CAPACITANCE

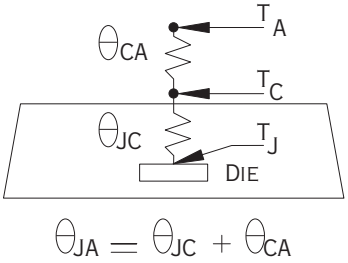
The Tristate function on pin 1 has a built-in pull-up resistor typical 50kΩ, so it can be left floating or tied to Vdd without deteriorating the electrical performance.

15-Day Aging of a QT122L10S-200MHz





(Figure 1)



(Figure 2)

Jitter And Phase Noise

As data rate increases, effect of jitter becomes critical with its budget tighter. Jitter is the deviation of a timing event of a signal from its ideal position. Jitter is complex and is composed of both random jitter (RJ) and deterministic jitter (DJ) components.
Random Jitter (RJ) is theoretically unbounded and Gaussian in distribution, while Deterministic Jitter (DJ) is bounded and does not follow any predictable distribution.

Q-Tech utilizes the EZJIT Plus jitter analysis software with Noise reduction software that supports Agilent Infinium real-time oscilloscope. Measure at its maximum sampling rate 40Gs/s and memory depth, we can separate the signal's aggregate total jitter into Random Jitter (RJ) and Deterministic Jitter (DJ).

Since Random Jitter is unbounded and Gaussian in style, the Total Jitter is a function of Bit Error Rate (BER).

TJ = RJ + DJ

Where:

TJ = RJ(rms) x 2α + DJ(p-p)

BER	α
10E-3	3.1
10E-6	4.75
10E-9	6
10E-12	7.0

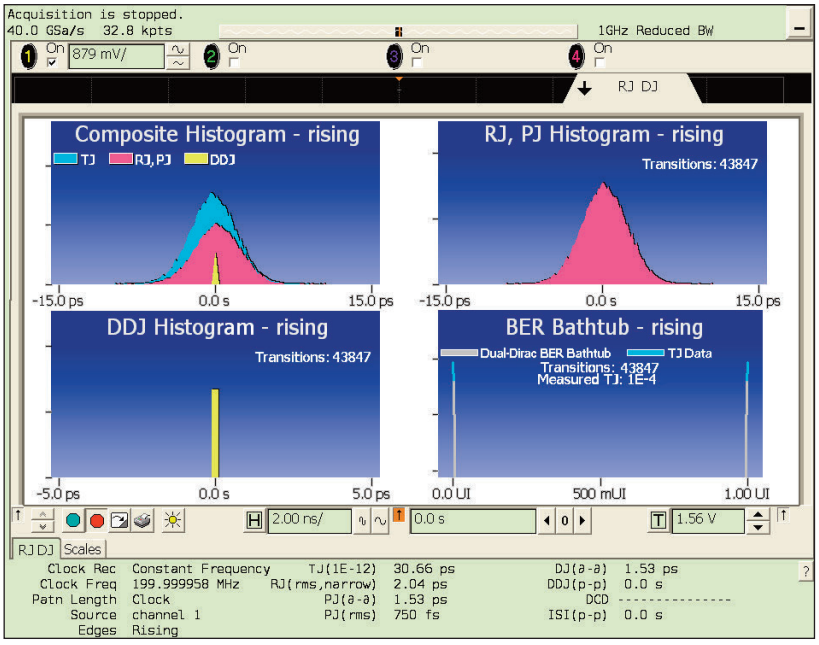


Figure 1: Jitter Analysis of a QT128L10S-200MHz

Figure 2: Jitter Analysis of a QT192LD9S-125MHz

Typical Jitter at BER=10E-12

Frequency	DJ (p-p) ps	RJ (rms) ps	TJ (ps)
22.118MHz	31	3.36	78.9
100MHz	1.61	1.99	21.1
125MHz	1.34	1.23	18.9
200MHz	1.53	2.04	30.7

Typical Phase Noise

Frequency	10Hz	100Hz	1kHz	10kHz	100kHz	1MHz	Phase Jitter (ps) *
22.118MHz	-90	-125	-150	-157	-162	-162	0.151
100MHz	-76	-101	-128	-140	-143	-149	0.120
125MHz	-74	-101	-131	-143	-145	-150	0.118
200MHz	-73	-99	-124	-134	-145	-148	0.121

(*) Integrated from 1kHz to 20MHz

Phase Noise and Phase Jitter Integration

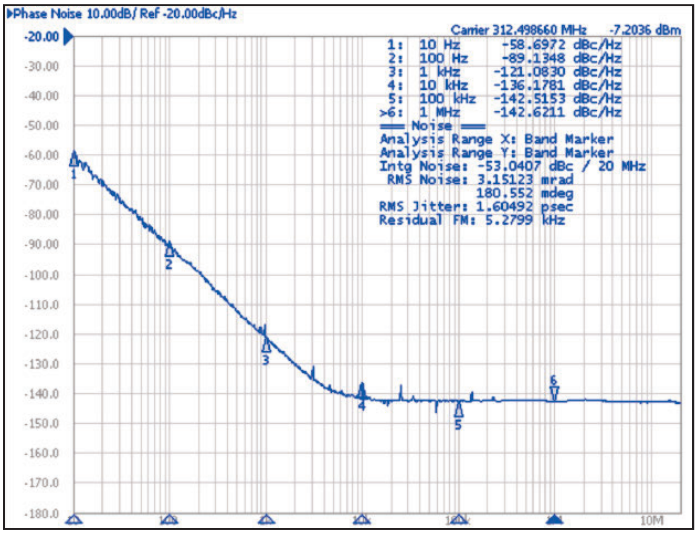
Phase noise is measured in the frequency domain, and is expressed as a ratio of signal power to noise power measured in a 1Hz bandwidth at an offset frequency from the carrier, e.g. 10Hz, 100Hz, 1kHz, 10kHz, 100kHz, etc. Phase noise measurement is made with an Agilent E5052A Signal Source Analyzer (SSA) with built-in outstanding low-noise DC power supply source. The DC source is floated from the ground and isolated from external noise to ensure accuracy and repeatability.

In order to determine the total noise power over a certain frequency range (bandwidth), the time domain must be analyzed in the frequency domain, and then reconstructed in the time domain into an rms value with the unwanted frequencies excluded. This may be done by converting L(f) back to Sφ(f) over the bandwidth of interest, integrating and performing some calculations.

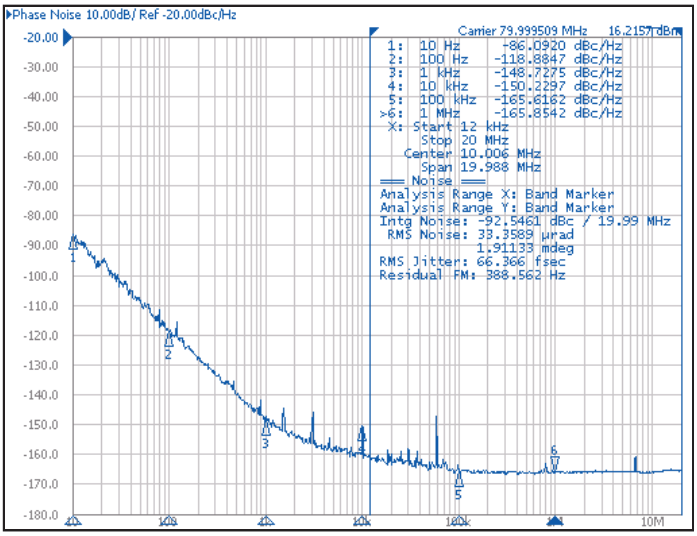
Symbol	Definition
$\int \mathcal{L}(f)$	Integrated single side band phase noise (dBc)
$S\varphi\ (f)=(180/\Pi)x\sqrt{2\int \mathcal{L}(f)df}$	Spectral density of phase modulation, also known as RMS phase error (in degrees)
RMS jitter = Sφ (f)/(fosc.360°)	Jitter(in seconds) due to phase noise. Note Sφ (f) in degrees.

The value of RMS jitter over the bandwidth of interest, e.g. 10kHz to 20MHz, 10Hz to 20MHz, represents 1 standard deviation of phase jitter contributed by the noise in that defined bandwidth.

Figure below shows a typical Phase Noise/Phase jitter of a QT193NW10M, 2.5Vdc, 312MHz and QT178AC9A, 5.0Vdc, 80MHz clock at offset frequencies 10Hz to 1MHz, and phase jitter integrated over the bandwidth of 12kHz to 1MHz.



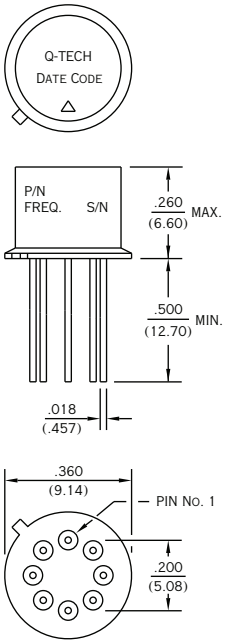
QT193NW10M, 2.5Vdc, 312MHz



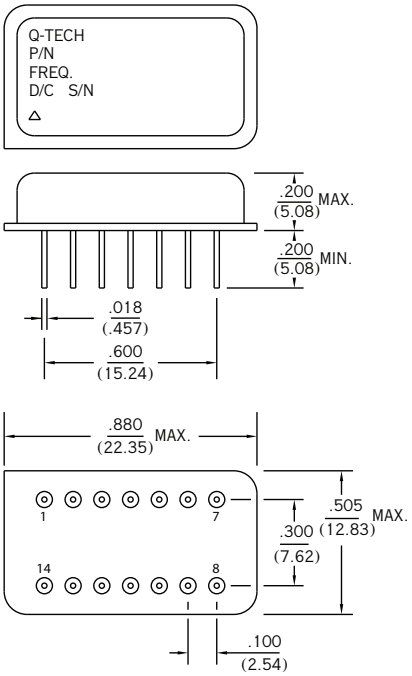
QT178AC9A, 5.0Vdc, 80MHz

Package Outline - Dimensions are in inches (mm)

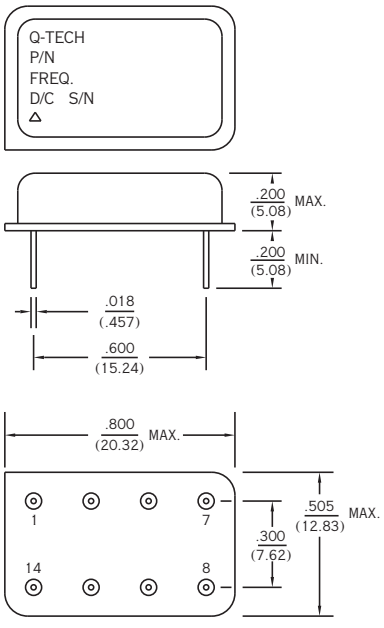
QT101



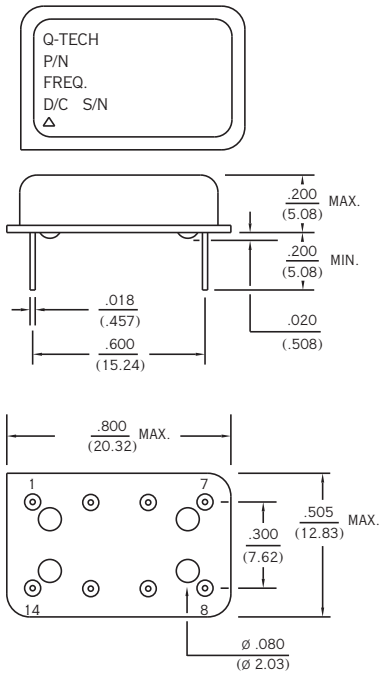
QT106



QT141

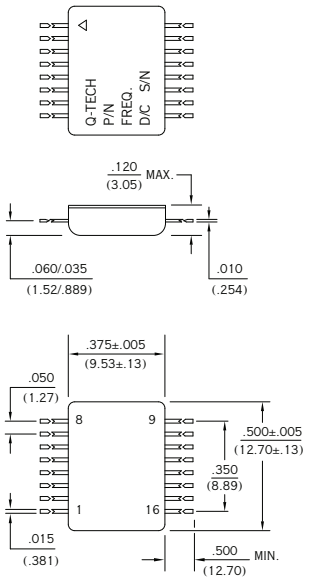


QT142

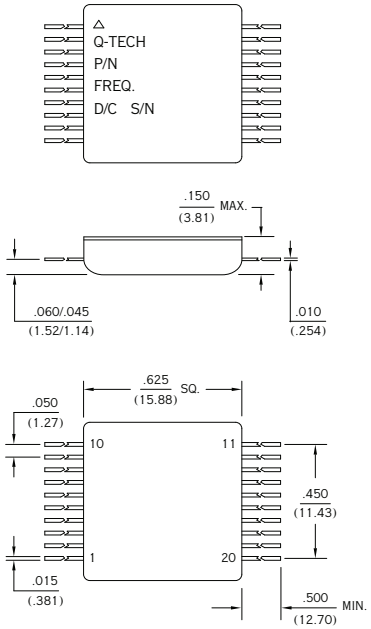


Package Outline - Dimensions are in inches (mm) (Continued)

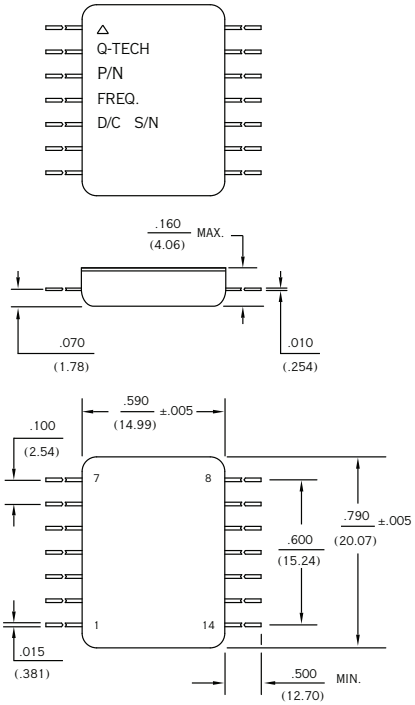
QT122



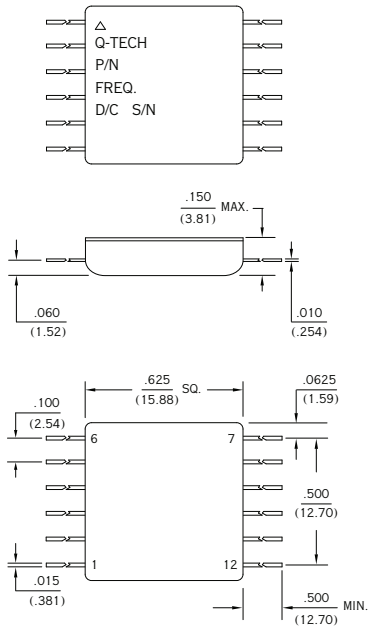
QT125



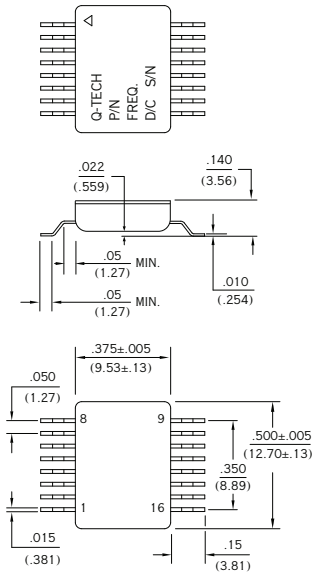
QT126



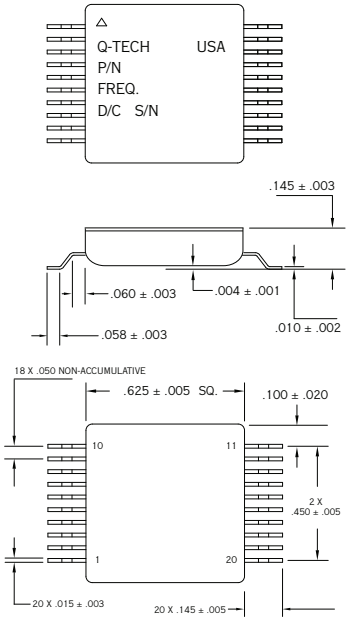
QT130



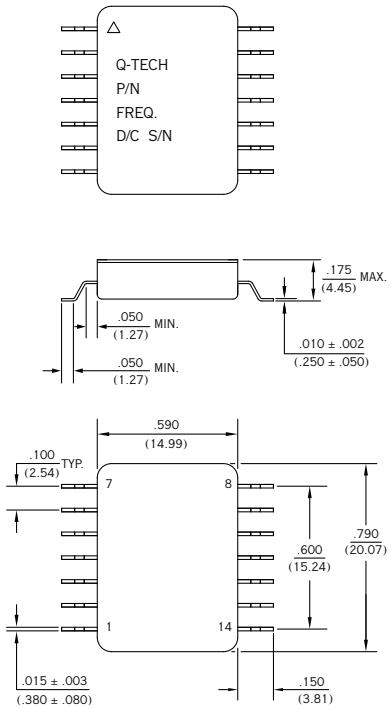
QT128



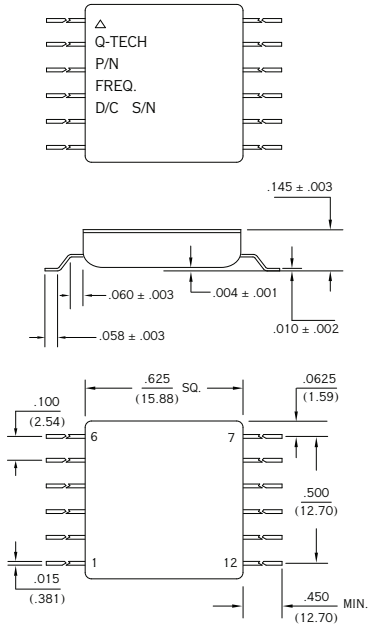
QT127



QT129

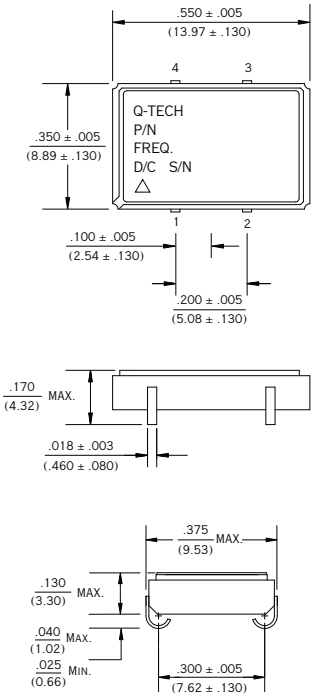


QT131

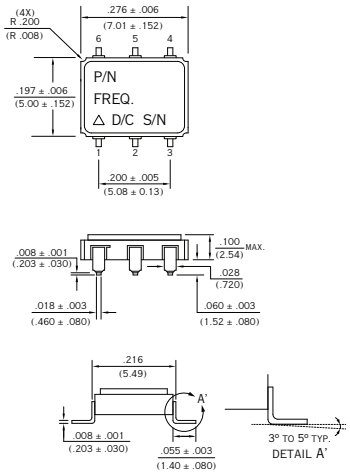


Package Outline - Dimensions are in inches (mm) (Continued)

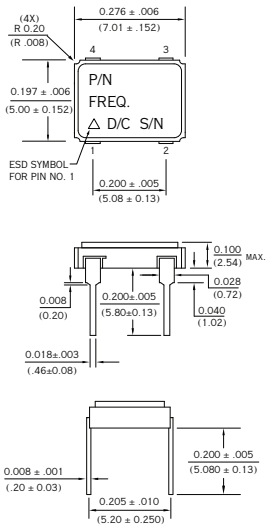
QT178



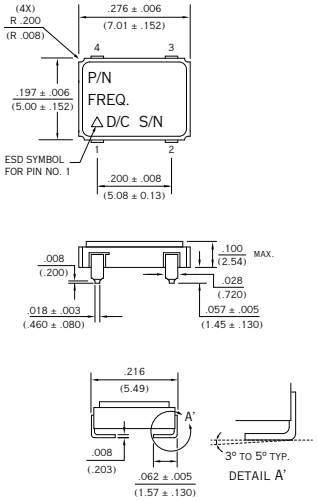
QT180



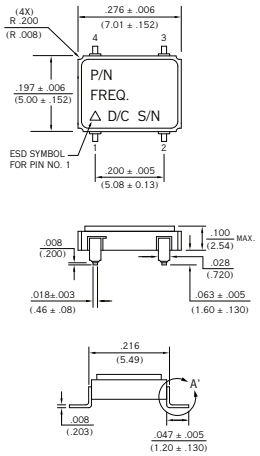
QT181



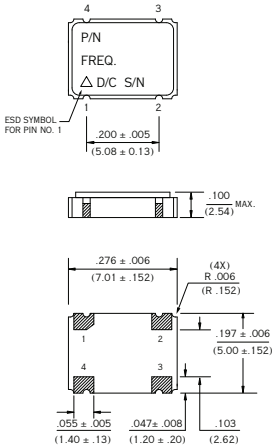
QT182



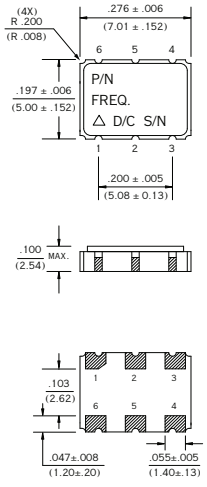
QT183



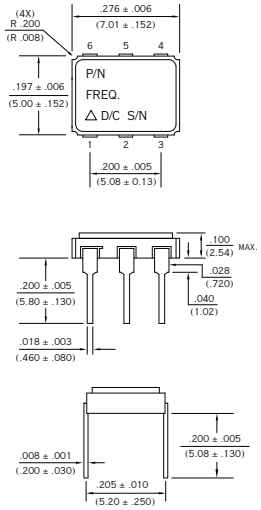
QT184



QT185

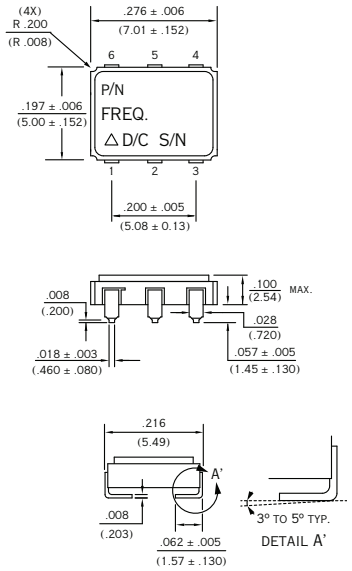


QT186

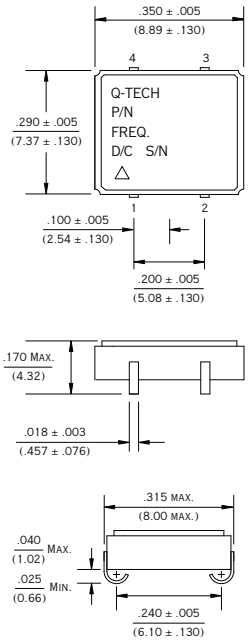


Package Outline - Dimensions are in inches (mm)
(Continued)

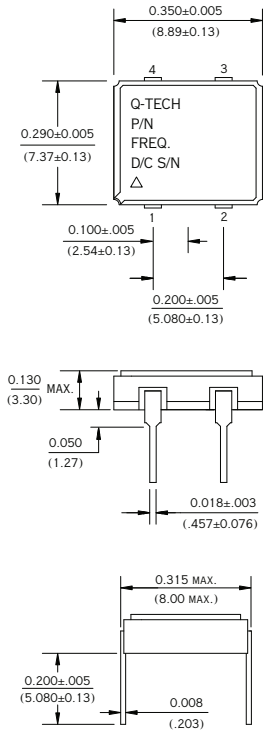
QT187



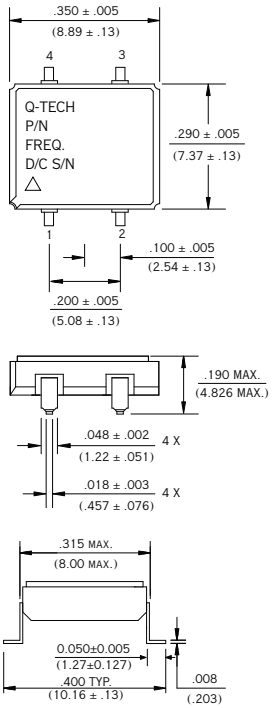
QT188



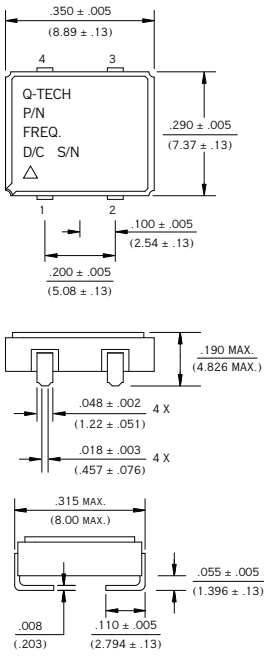
QT189



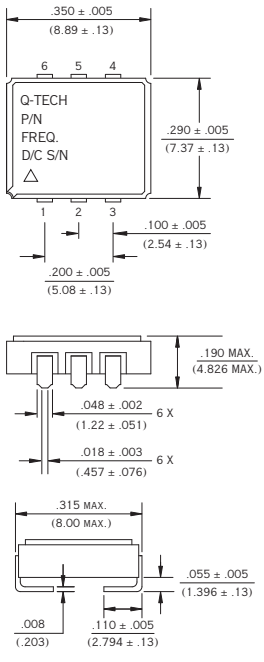
QT190



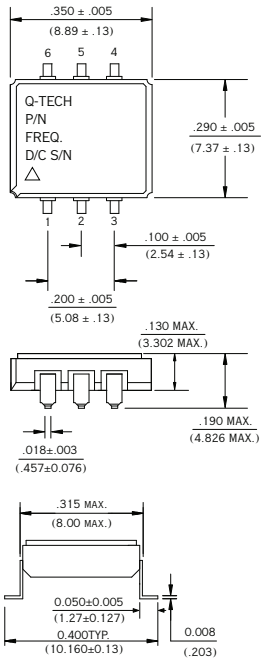
QT192



QT193



QT194



QT#	Vcc	GND	Case	Output	E/D or N/C	Equivalent MIL-PRF-55310 Configuration	LVDS and LVPECL Outputs
 QT101	8	4	4	5	2	/9 = QT1T	
 QT106	14	7	7	8	1	/16 = QT6T /26A = QT6HC	
 QT141	14	7	7	8	1	/26B = QT41HC	
 QT142	14	7	7	8	1	N/A	
 QT122	8	9	9	10 (CMOS, TTL) 10 & 11 (LVDS, LVPECL)	7 7	N/A	Pin 10 OutN (-) Pin 11 Out (+)
 QT128	8	9	9	10 (CMOS, TTL) 10 & 11 (LVDS, LVPECL)	7 7	N/A	Pin 10 OutN (-) Pin 11 Out (+)
 QT125	13	10	10	11 (CMOS, TTL) 11 & 12 (LVDS, LVPECL)	12 8	/21 = QT25T	Pin 11 OutN (-) Pin 12 Out (+)
 QT127	13	10	10	11 (CMOS, TTL) 11 & 12 (LVDS, LVPECL)	12 8	N/A	Pin 11 OutN (-) Pin 12 Out (+)
 QT126	14	7	7	8	6	N/A	
 QT130/ QT131	12	6	6	7 (CMOS, TTL) 7 & 8 (LVDS, LVPECL)	8 5	N/A	Pin 7 OutN (-) Pin 8 Out (+)
 QT129	14	7	7	8	6	N/A	
 QT178	4	2	2	3	1	/27 = QT78HCD /28 = QT78TD /30 = QT78LD	
 QT180	6	3	3	4 (CMOS) 4 & 5	1	N/A	Pin 4 OutN (-) Pin 5 Out (+)
 QT181	4	2	2	3	1	N/A	
 QT182	4	2	2	3	1	N/A	
 QT183	4	2	2	3	1	N/A	
 QT184	4	2	2	3	1	N/A	
 QT185	6	3	3	4 (CMOS) 4 & 5	1	N/A	Pin 4 OutN (-) Pin 5 Out (+)
 QT186	6	3	3	4 (CMOS) 4 & 5	1	N/A	Pin 4 OutN (-) Pin 5 Out (+)
 QT187	6	3	3	4 (CMOS) 4 & 5	1	N/A	Pin 4 OutN (-) Pin 5 Out (+)
 QT188	4	2	2	3	1	/33 = QT88HCD /34 = QT88LD /35 = QT88ND	
 QT189	4	2	2	3	1	N/A	
 QT190	4	2	2	3	1	N/A	
 QT192	4	2	2	3	1	/37 = QT92HCD /38 = QT92LD /39 = QT92ND	
 QT193	6	3	3	4 (CMOS, TTL) 4 & 5 (LVDS) 4 & 5 (LVPECL)	1	N/A	Pin 4 OutN (-) Pin 5 Out (+)
 QT194	6	3	3	4 (CMOS, TTL) 4 & 5 (LVDS) 4 & 5 (LVPECL)	1	N/A	Pin 4 OutN (-) Pin 5 Out (+)

Package Information

QT101
- Package material (header and leads): Kovar
- Lead finish: Gold Plated – 50µ ~ 80µ inches
  Nickel Underplate – 100µ ~ 250µ inches
- Cover: Pure Nickel Grade A
- Package to lid attachment: Resistance weld
- Weight: 2.0g typ., 4.96g max.

QT106, QT141, QT142
- Package material (header and leads): Kovar
- Lead finish: Gold Plated – 50µ ~ 80µ inches
  Nickel Underplate – 100µ ~ 250µ inches
- Package to lid attachment: Resistance weld
- Cover: (DIP-14): Pure Nickel Grade A
- Weight: (DIP-14): 3.4g typ.,14.2g max.

QT122, QT125, QT126, QT127, QT128, QT129, QT130, QT131:
- Package material (Header and Leads): Kovar
- Lead finish: Gold Plated – 50µ ~ 80µ inches
  Nickel Underplate – 100µ ~ 250µ inches
- Cover: Kovar, Gold Plated – 50µ ~ 100µ inches
  Nickel Underplate – 70µ ~ 90µ inches
- Package to lid attachment: Seam weld
- Weight: 2.0g typ., 4.0g max.

QT178, QT180, QT181, QT182, QT183, QT184, QT185, QT186, QT187 QT188, QT189, QT190, QT192, QT193, QT194
- Package material: 90% AL2O3
- Lead material: Kovar
- Lead finish: Gold Plated: 50µ ~ 80µ inches
  Nickel Underplate: 100µ ~ 250µ inches
- Weight: QT178: 1.1g typ., 3.0g max.
  QT180, QT181, QT182, QT183, QT184, QT185, QT186, QT187 QT188, QT189, QT190, QT192, QT193, QT194: .6g typ., 3.0g max.

Packaging Options

QT101, QT106, QT141, QT142
- Standard packaging in black foam

QT122, QT125, QT126, QT127, QT128, QT129, QT130, QT131
- Standard packaging in a locked anti-static cardboard

QT178, QT180, QT181, QT182, QT183, QT184, QT185, QT186, QT187 QT188, QT189, QT190, QT192, QT193, QT194
- Standard packaging in anti-static plastic tube (60pcs/tube)
- Tape and Reel is available for an additional charge.

Specifications subject to change without prior notice.

QCI Per MIL-PRF-38534, CLASS K (Modified)

Table VII
Group B Inspection (Note 1)

Subgroup	Test Description	MIL-STD-883		Quantity / (Accept No.)
		Method	Condition	
1	Physical Dimensions	2016	-	2 (0)
2	Particle Impact Noise Detection (Note 2)	2020	B	15 (0)
3	Resistance to Solvents	2015	-	3 (0)
4	Internal Visual and Mechanical	2014	-	1 (0)
5	Bond Strength (Note 3)	2011	C or D	2 (0)
6	Die Shear Strength (Note 4)	2019	-	2 (0)
7	Solderability (Note 5)	2003	Solder Temperature: 245 ±5º C	1 (0)
8	Seal; Fine Leak and Gross Leak (Note 6)	1014	A1 or B1 & C, B2, or B3	4 (0)
9	ESD Classification (Note 7)	3015	-	4 (0)

NOTES:
1. Non catastrophic screening test rejects may be used for Group B.
2. To be omitted. Performed during screening, see Table I.
3. Subgroup 5 shall be performed in accordance with the Group B bond strength requirements of MIL-PRF-38534. This test may be performed in-process anytime prior to cover seal.
4. Die shear test samples shall not be the same units as subjected to bond pull. Die shear specimens shall not be exposed to the 300ºC preconditioning used for the bond strength test.
5. Solder temperature shall be 245 ±5ºC.
6. Subgroup 8, the fine and gross leak tests are being done during screening, see Table I.
7. Subgroup 9, the ESD classification test, is not required. The hybrid has been classified as ESDS Class 1C (i.e., Electrostatic voltage = 1999V) and shall be marked accordingly.

Table VIII
Group C Inspection

Subgroup	Test Description	MIL-STD-883		Quantity / (Accept No.)
		Method	Condition	
1	External Visual	2009		5 (0) (Note 1, 3)
	Temperature Cycling	1010	C, 20 Cycles	
	Constant Acceleration	2001	A, Y_1 Axis	
	Seal (fine & gross leak)	1014	A1 or B1 & C, B2, or B3	
	Radiographic Inspection	2012		
	Visual Examination			
	End Point Electricals (Note 2)			
2	End Point Electricals (Note 2) Steady State Life End Point Electricals (Note 2)	1005	1000 hours at 125ºC	5 (0) (Note 3)
3	Internal Gas Analysis	1018		3 (0) or 5 (1)

NOTES:
1. Five units shall be used for Group C inspection based on limited usage acquisition requirements of MIL-PRF-38534.
2. End point electrical shall be as specified for the applicable device specification.
3. Subgroup 1 specimens shall be used for subgroup 3 testing, but not recommended for subgroup 2 testing.

QCI Per MIL-PRF-38534, CLASS K (Modified)
(continued)

Table IX
Group D Inspection

Subgroup	Test Description	MIL-STD-883		Quantity / (Accept No.)
		Method	Condition	
1	Thermal Shock	1011	C	5 (0)
	Stabilization Bake	1008	1 hour at 150ºC	5 (0)
	Lead Integrity	Per MIL-PRF-55310, test method is dependent on package type		1 (0)
	Seal (fine and gross leak)	1014	A1 or B1 & C, B2, or B3	5 (0)

NOTES

1. Group D inspection is not required when package evaluation has been performed at incoming inspection.

QCI Per MIL-PRF-55310

Table X
Group C Inspection

Subgroup	Test Description	Test Method	Quantity (Accept No.)
1	Vibration (Sinusoidal, Non-Operating) Shock (Specified Pulse, Non-Operating) Random Vibration (Non-Operating)	MIL-STD-202, Method 204 **(Note 3)** MIL-STD-202, Method 213, Condition I MIL-STD-883, Method 2026, Condition I-J	8 (0)
2	Thermal Shock Ambient Pressure (non-operating) Ambient Pressure (operating) Storage Temperature	MIL-STD-202, Method 107, Condition B MIL-PRF-55310, Paragraph 4.8.46.1 MIL-STD-202, Method 105, Condition C MIL-PRF-55310, Paragraph 4.8.47	2 (0) (Level S) or 4 (0) (Level B) **(Note 5)**
3	Resistance to Solder Heat Moisture Resistance Salt Atmosphere	MIL-STD-202, Method 210 **(Note 3)** MIL-STD-202, Method 106 MIL-STD-883, Method 1009, Condition A	2 (0)
4	Terminal Strength (Leaded Packages) Terminal Strength (Leadless Packages) Resistance to Solvents	MIL-STD-202, Method 211 **(Note 3)** MIL-STD-883, Method 2004, Condition D MIL-STD-202, Method 215	2 (0)
5	End Point Electricals (Note 4) Life Test End Point Electricals (Note 4)	MIL-STD-883, Method 1005 (1000 Hours at 125ºC)	2 (0) (Level S) **(Note 5)**

NOTES

1. Eight (8) sample units shall be selected from inspection lots which have passed quality conformance inspection. Group C may be completed with a minimum sample size of four (4) units as specified by the qualifying activity.
2. All test conditions are in accordance with MIL-PRF-55310.
3. Test Condition is dependent on package type.
4. Measure current, frequency, and output waveform at 23ºC and temperature extremes. Frequency after life test shall be within ±10ppm of pre-life frequency.
5. When ordered with Screening Code 'B' only, Subgroup 2 shall be tested on 2 units and Subgroup 5 (Life Test) is not required.

Revision History

ECO	REV	REVISION SUMMARY	PAGE	DATE
9625	U	Change titles of Table IV-b and V-b to "Group A Inspection 100%"	15 & 17	06/26/2019
		Change max frequency to 250MHz (was 350MHz)	All	
		Change name of Table IV-c to 'Qualification Test Requirements' (was 'Additional Electrical Measurements')	15	
		Revise/Add notes under table IV-c	15	
		Add QT130 and QT131 package information	5, 29, 32, 33	
		Revise notes under several screening/QCI tables to clear up wording and references	8 - 17	
		Update thickness and correct dimensions on all 5x7mm package outlines. Thickness was .079 (2.00), is now .100 (2.54) inches (mm)	30	
		Fix QT101 Markings to the actual format used	28	
		Table I, Frequency Aging 30 Days: Remove limits in Comments column. Specifications depend on detail specification.	8	
		Revise Temperature Code Note (***) for 5x7mm oscillators	1	
		Revised QT127 outline	29	
		Add Notes for Differential Output Voltage tests (LVDS) to Test Matrices	9 - 18	
		Add note for Aging after Life Test under Table I-b	9	
		Revise BiCMOS Electrical Characteristics table to add 1.8Vdc for frequencies of 40 - 100MHz)	20	
		Add new Electrical Characteristics table for 1.8V & 2.5V CMOS specifications for frequencies of 450kHz to 40MHz	21	
		Fix Enable/Disable Pinout for CMOS QT122/QT128	32	
		Update requirements for MIL-PRF-55310 Screening options (Options A and C) and Group C to match MIL-PRF-55310 Revision F	10 - 13, 35	
		Add /36 and /40 reference part number to 'equivalent' list	1	
		Update Environmental Specifications Table	24	
		Update MIL-PRF-38534, Class K Group B Table VII: Resistance to Solvents quantity changed to 3 (0), was 4 (0)	34	
11153	V	Add Random Vibration to screening options 'A' and 'C'	7, 10, 12	08/06/2020
		Add check mark to option B, Group A QCI in Screening Options Summary Table	7	
		Table V, Note 1: 100% Group A QCI per Table V-b is now always required/tested when ordered (removed 'when specified on the PO' verbiage).	16	
		Correct test method for Random Vibration in Table X - MIL-PRF-55310 Group C	35	
		Fix QT122 and QT128 pinouts	32	
		Add 5x7 Aging specifications on Electrical Characteristics tables	19, 20, 22, 23	
		Modify VIH and VIL spec to accomodate all voltages	20, 21	
		Change/add Frequency Voltage Tolerance for different package types/frequencies across all electrical characteristics tables	19 - 23	

ECO	REV	REVISION SUMMARY	PAGE	DATE
14507	W	Update page numbers Update Q-Tech Address and Fax Number	All	04/27/2022
		Add Paragraph 3.5.4.1 Scanning Electron Microscopy Add SEM Note to BiCMOS Electrical Characteristics tables	3, 21, 23, 24	
		Add notes to clarify voltage, logic, and frequency options for all package types	5, 6, 7	
		Fix QT186 outline to correct pin number callouts	31	
		Add note to screening table for Fine/Gross Leak: Conditions A1 and C are used if B1 and B2 are not purchased by the customer.	11, 13	
		Add note to MIL-PRF-55310 Group A Tables: Testing performed as part of Final Electrical in screening is not required to be repeated as part of Group A.	10, 12, 14, 18	
		Modify 5x7mm package aging specification for frequencies up to 44MHz	20	
		Modify 5x7mm package rise and fall time frequency ranges	20	
		Clarify Duty Cycle and Rise and Fall Time test conditions for CMOS and TTL	20	
		Frequency/Voltage Tolerance modified for 5V and 3.3V in DIP and Flat Packages for frequencies between 15kHz ≤ F ≤ 27MHz and 36MHz ≤ F ≤ 85MHz	20	
N/A	X	Revision not used	N/A	N/A
16689	Y	Table X: Update Note 1, change MIL-PRF-55310 Group C standard quantity to 8 units	36	05/10/2023
		Updating aging specification for 5x7mm packages	20, 21, 23, 24	
		Updating Frequency/Voltage tolerance specification	20, 21	