Description

The QT2024 is an I²C-bus serial interface conforming, high-precision real-time clock (RTC) IC with a built-in 32.768kHz crystal oscillator circuit. In addition to clock and calendar functions, it is equipped with an alarm interrupt function, fixed-cycle timer interrupt function, time update interrupt function, clock output function, and supply voltage detection function.

Features

- Made in the USA
- ECCN: EAR99
- +3.3Vdc operation
- 32.768kHz square wave output
- Wide operating temperature (-55°C to +185°C)
- Very good stability
- Low current 90µA at +25°C
- I²C-bus serial interface corresponding to fast data transfer: 400kHz fast-mode compatible.
- Clock function: hour, minute, second
- Calendar function with auto leap year adjustment: year, month, day,day of week
- Alarm interrupt function: day day of week, hour, minute
- Low minimum Standby (Timekeeping) Voltage at 2.2V
- Buffered Clock Output
- Three Independent Interrupt Modes
  - Alarm
  - Fix-cycle timer
  - Time update

Applications

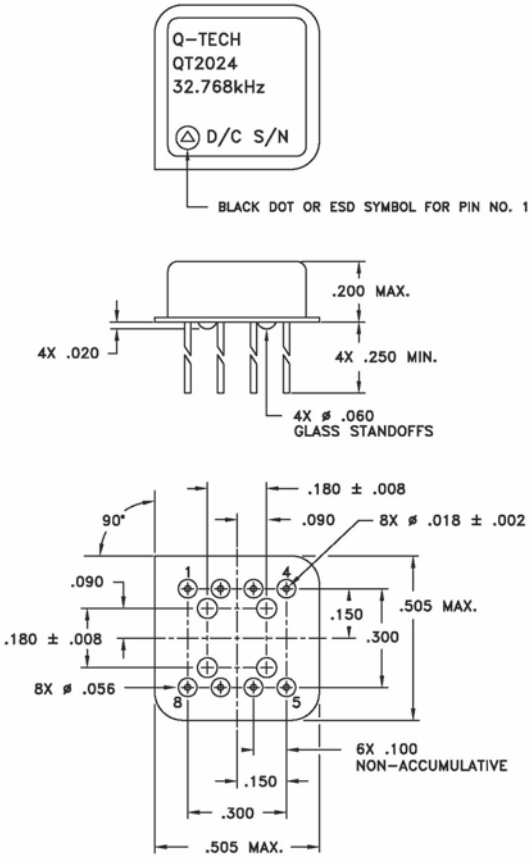
- Data logging
- Real Time Clock functions

Electrical Parameters

Parameters	Rating
Output freq. (Fo)	**32.768kHz**
Supply voltage (Vdd)	3.3Vdc ± 10%
Maximum Applied Voltage (Vdd max.)	+5Vdc
Freq. stability (ΔF/ΔT)	See Option codes
Operating temp. (Topr)	See Option codes
Storage temp. (Tsto)	-62ºC to + 150ºC
Operating supply current (Idd) (No Load)	65µA Typ. at 25ºC 90µA max, V_{DD} = 3.3Vdc, 70µA max, V_{BdATT} = 2.3Vdc
Symmetry (50% of ouput waveform)	45/55% max.
Rise and Fall times (Tr/Tf) (with typical load)	20 ns typ. 70 ns max. (Measured from 10% to 90%)
Output Load	15pF // 10kΩ
Start-up time (Tstup)	10ms max.
Output voltage (Voh/Vol)	Voh = 2.2Vdc min. Vol = 0.8V max.
Output Current (Ioh/Iol)	± 1mA min.

Package Outline and Pin Connections

Dimensions are in inches (mm)



Pin No.	Pin Name	Description
1	OSC OUT	32.768kHz Oscillator output test point
2	CLKOE	CLKOUT output control enable input pin (clock output when HIGH, Hi-Z when LOW).
3	INTN	1Hz signal, alarm interrupt signal, fixed-cycle timer interrupt and time update interrupt signal, N-channel open-drain output.
4	GND	Ground pin : Connect this pin to ground
5	CLKOUT	Clock output (CMOS output with output state controlled by CLKOE.
6	SCL	I²C-bus serial interface clock input.
7	SDA	I²C-bus serial interface daqta input/output (Address, data and acknowledge bit input/output, in sync with the SCL clock input. N-channel open-drain output.)
8	VDD	The positive power-supply pin: Connect this pin to the power supply

Package Information

- Package material (header and leads): Kovar
- Lead finish: Gold Plated – 50µ ~ 80µ inches
  Nickel Underplate – 100µ ~ 250µ inches
- Package to lid attachment: Resistance weld
- Cover: Pure Nickel Grade A or Stainless Steel
- Weight: 3.4g typ.,14.2g max.

Ordering Information

(Sample part number)

QT2024C8M-32.768kHz

Q	T	2024	L	80	M	-	32.768kHz

Solder Dip Option:
T = Standard
S = Solder Dip (*)
G = Solder Dip (*)

Part Number

Logic & Supply Voltage:
L = LVHCMOS +3.3V

Output Frequency

Screening Option:
Blank = No Screening
M = Per MIL-PRF-55310, Level B

Operating Temperature Option:

80	= ±40ppm	@ 0ºC to +175ºC	(Operable up to + 185ºC)
81	= ±75ppm	@ 0ºC to +175ºC	(Operable up to + 185ºC)
82	= ±40ppm	@ -20ºC to +175ºC	(Operable up to + 185ºC)
83	= ±75ppm	@ -20ºC to +175ºC	(Operable up to + 185ºC)
84	= ±75ppm	@ 0ºC to +185ºC	
85	= ±75ppm	@ -20ºC to +185ºC	
86	= ±100ppm	@ -20ºC to +185ºC	
87	= ±150ppm	@ -20ºC to +185ºC	
88	= ±200ppm	@ -20ºC to +175ºC	(Operable up to + 185ºC)
89	= ±250ppm	@ -40ºC to +175ºC	(Operable up to + 185ºC)
90	= ±200ppm	@ -40ºC to +185ºC	
91	= ±250ppm	@ -40ºC to +185ºC	
92	= ±250ppm	@ -55ºC to +185ºC	

For Non-Standard requirements, contact Q-Tech Corporation at Sales@Q-Tech.com

Packaging Options

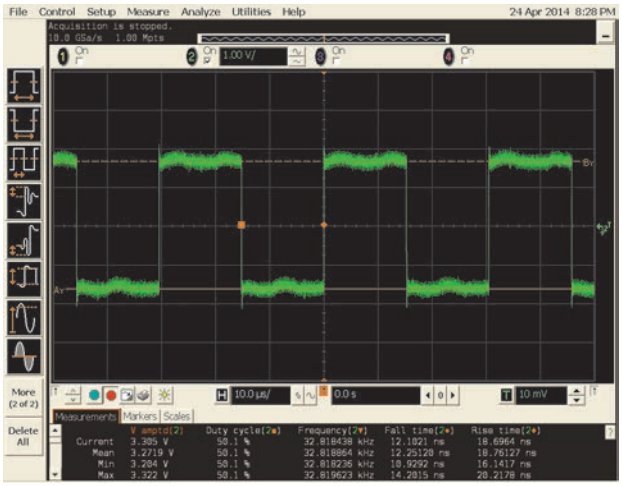
- Standard packaging in black foam
- Optional anti-static plastic tube

Other Options Available For An Additional Charge

- Lead forming available. Please contact for details.
- Lead trimming
- P. I. N. D. test (MIL-STD 883, Method 2020)

(*) Hot Solder Dip options for an additional cost:
S = Sn60/Pb40 per MIL-PRF 55310
G = Lead free Alloy SAC305 (96.5% Sn, 3% Ag, 0.5% Cu)

Output Waveform (Typical)



Startup Time

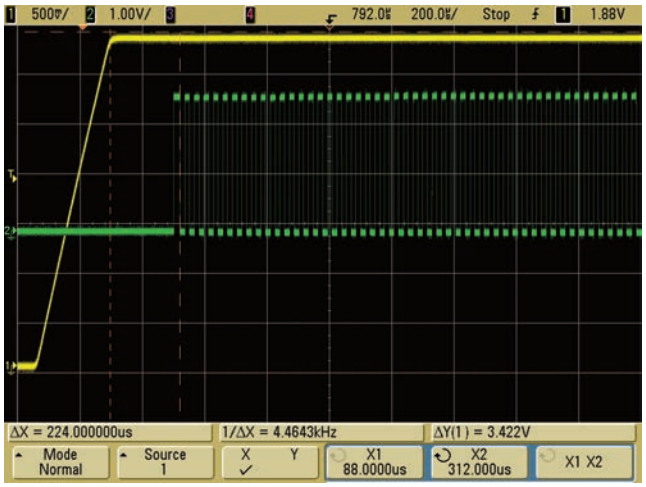
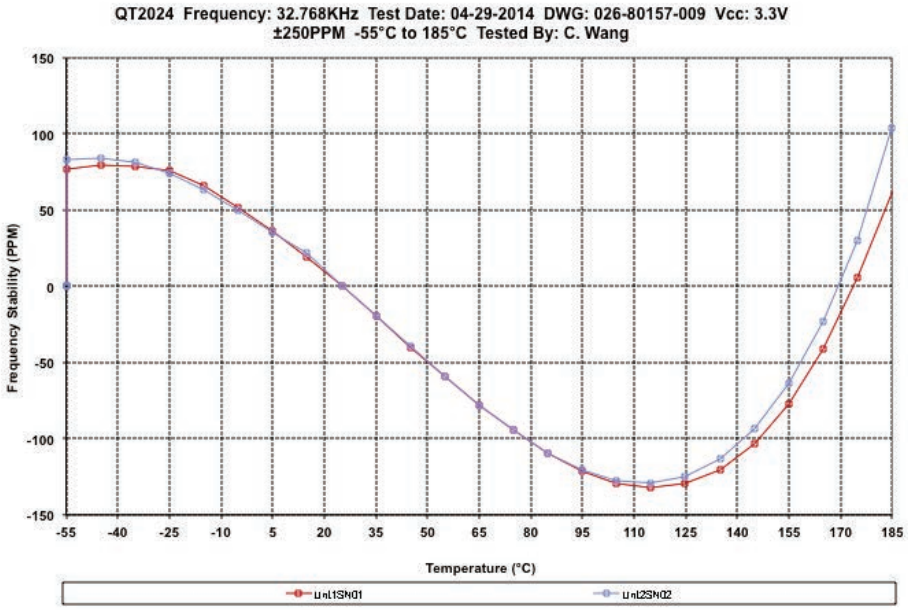


Chart vs. Nominal



AC Characteristics 1 (I^2C-bus Serial Interface: Time control register access)

V_{DD}=1.5 to 5.5V, V_{SS}=0V, T_a= -40 to +85°C unless otherwise noted.

Parameter	Symbol	Conditions	Rating			Unit
			Min	Typ	Max	
SCL clock frequency	f_{SCL}	-	-	-	400	kHz
START condition setup time	$t_{SU;STA}$	-	0.6	-	-	µs
START condition hold time	$t_{HD;STA}$	-	0.6	-	-	µs
Data setup time	$t_{SU;DAT}$	-	100	-	-	ns
Data hold time	$t_{HD;DAT}$	-	0	-	900	ns
STOP condition setup time	$t_{SU;STO}$	-	0.6	-	-	µs
Bus free time between START and STOP conditions	t_{BUF}	-	1.3	-	-	µs
SCL L-level pulse width	t_{LOW}	-	1.3	-	-	µs
SCL H-level pulse width	t_{HIGH}	-	0.6	-	-	µs
SCL, SDA rise time	t_r	20% → 80%	-	-	0.3	µs
SCL, SDA fall time	t_f	80% → 20%	-	-	0.3	µs
Maximum bus spike time	t_{SP}	-	-	-	50	ns
Bus line load capacitance	C_b	$V_{DD} \geq 1.8V$	-	-	400	pF
		$V_{DD} < 1.8V$	-	-	50	

AC Characteristics 2 (CLKOUT Output)

V_{DD} = 1.3 to 5.5V, V_{SS}= 0V, T_a = -40 to +85°C unless otherwise noted

Parameter	Symbol	Conditions		Rating			Unit
				Min	Typ	Max	
CLKOUT duty	Duty	C_{LOUT}=15pF, 0.5V_{DD} threshold, CL setting = 100h to 7FFh*1		40	50	60	%
CLKOUT rise time	t_{rC}	C_{LOUT}=15pF, 20% → 80%	V_{DD} = 1.8 to 5.5V	-	-	70	ns
			V_{DD} = 1.5 to 5.5V	-	-	180	
			V_{DD} = 1.3 to 5.5V	-	-	1100	
CLKOUT fall time	t_{fC}	C_{LOUT}=15pF, 80% → 20%	V_{DD} = 1.8 to 5.5V	-	-	70	ns
			V_{DD} = 1.5 to 5.5V	-	-	180	
			V_{DD} = 1.3 to 5.5V	-	-	1100	

*1. C_{LOUT} is the IC external load capacitance connected to CLKOUT.
The CL setting represents the internal crystal oscillator circuit load capacitance (C_L).

Time Control Register Table

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00h	SEC	-	S40	S20	S10	S8	S4	S2	S1
01h	MIN	-	M40	M20	M10	M8	M4	M2	M1
02h	HOUR	-	-	H20	H10	H8	H4	H2	H1
03h	WEEK	-	-	-	-	-	W4	W2	W1
04h	DAY	-	-	D20	D10	D8	D4	D2	D1
05h	MONTH	-	-	-	MO10	MO8	MO4	MO2	MO1
06h	YEAR	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
07h	MIN Alarm	AE	MA40	MA20	MA10	MA8	MA4	MA2	MA1
08h	HOUR Alarm	AE	RAM	HA20	HA10	HA8	HA4	HA2	HA1
09h	WEEK Alarm	AE	WA6	WA5	WA4	WA3	WA2	WA1	WA0
	DAY Alarm		RAM	DA20	DA10	DA8	DA4	DA2	DA1
0Ah	Timer Counter	T128	T64	T32	T16	T8	T4	T2	T1
0Bh	Select Register	TCS1	TCS0	CFS1	CFS0	TSS1	TSS0	AS	UTS
0Ch	Flag Register	-	-	VDHF	VDLF	-	TF	AF	UTF
0Dh	Control Register	RESE	TEST	RAM	FIE	TE	TIE	AIE	UTIE

* The register values are undefined when power is first applied; ensure the device is configured before use.
  Note that the TCS1, TCS0, CFS1, CFS0, TEST, FIE, TE, TIE, AIE, and UTIE bits are reset to "0", and the VDLF bit is set to "1" when power is applied.
* Bits indicated by a hyphen "-" are read-only bits with read output value of "0".
* Only "0" data values can be written to the VDHF, VDLF, TF, AF, and UTF bits.
* The TEST bit is a reserved bit for manufacturer testing, and should always be set to "0" for normal operation.
* To access address 0Eh and 0Fh is prohibited for avoiding a malfunction. Don't access the address 0Eh and 0Fh.

Time and Calendar Register (Address 00h to 06h)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
00h	SEC	-	S40	S20	S10	S8	S4	S2	S1
01h	MIN	-	M40	M20	M10	M8	M4	M2	M1
02h	HOUR	-	-	H20	H10	H8	H4	H2	H1
03h	WEEK	-	-	-	-	-	W4	W2	W1
04h	DAY	-	-	D20	D10	D8	D4	D2	D1
05h	MONTH	-	-	-	MO10	MO8	MO4	MO2	MO1
06h	YEAR	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1

- Data format

  The time and calendar data is represented in BCD format.

- HOUR register

  The HOUR register contains the hour in 24-hour display mode.

- WEEK register

  The WEEK register increments using a 7-step up-counter: (W4W2W1) = (000) → (001) → … → (110) → (000). The logic tables for the (W4W2W1) bits for the day of the week are configurable by the user.

- YEAR register

  The YEAR register contains the last 2 digits of the western calendar year.

- Automatic leap year correction function

  The automatic leap year correction function corrects for leap years between 2000 and 2099.

Alarm Register (Address 07h to 09h)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
07h	MIN Alarm	AE	MA40	MA20	MA10	MA8	MA4	MA2	MA1
08h	HOUR Alarm	AE	RAM	HA20	HA10	HA8	HA4	HA2	HA1
09h	WEEK Alarm	AE	WA6	WA5	WA4	WA3	WA2	WA1	WA0
	DAY Alarm		RAM	DA20	DA10	DA8	DA4	DA2	DA1

This register specifies the alarm time using day of the week, day, hour, and minute settings. Address 09h specifies the day of the week or the day setting, selected by the AS (Alarm Select) bit in Address 0Bh. The AF (Alarm Flag) bit in Address 0Ch is set to "1" when a time is specified in the Alarm register.

Timer Counter Register (Address 0Ah)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0Ah	Timer Counter	T128	T64	T32	T16	T8	T4	T2	T1

This register specifies the count value of a down-counter used for fixed-cycle timer interrupts. The fixed-cycle timer source clock is specified using the TSS1 and TSS0 (Timer Source Clock Select) bits in Address 0Bh.
When the TE (Timer Enable) bit in Address 0Dh is changed from "0" to "1", the counter starts counting down from the specified count value. When the down-counter reaches zero, the TF (Timer Flag) bit in Address 0Ch is set to "1".
The down-counter continually repeats counting down from the specified count value while the TE bit is set to "1".

Select Register (Address 0Bh)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0Bh	Select Register	TCS1	TCS0	CFS1	CFS0	TSS1	TSS0	AS	UTS

• TCS (Temperature Compensation Select) bits

The TCS bits select the temperature compensation, operating interval.

Temperature compensation operates in sync with the clock register timing.

TCS1	TCS0	Temperature compensation operating interval
0	0	0.5 s
0	1	2 s
1	0	10 s
1	1	30 s

* When power is applied, TCS is reset to "00" and 0.5s temperature compensation operating interval is selected.

• CFS (CLKOUT Frequency Select) bits

The CFS bits select the CLKOUT output frequency.

CFS1	CFS0	CLKOUT output frequency
0	0	32.768 kHz
0	1	1024 Hz
1	0	32 Hz
1	1	1 Hz

* When power is applied, CFS is reset to "00" and 32.768kHz CLKOUT output frequency is selected.

• TSS (Timer Source Clock Select) bit

The TSS bits select the fixed-cycle timer source clock.

TSS1	TSS0	Timer source clock
0	0	4096 Hz
0	1	64 Hz
1	0	1 Hz
1	1	1/60 Hz

• AS (Alarm Select) bit

The AS bit selects day of week alarm or day alarm.

The alarm data in Address 09h is interpreted according to the following alarm setting.

AS	Alarm type
0	Day of week alarm
1	Day alarm

• UTS (Update Time Select) bit

The UTS bit selects the timing for generating time update interrupts.

UTS	Time update interrupt timing
0	Seconds digits update
1	Minutes digits update

Control Register (Address 0Dh)

Address	Function	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0Dh	Control Register	RESET	TEST	RAM	FIE	TE	TIE	AIE	UTIE

• RESET bit

RESET	Description
0	Normal operation
1	1 to 64Hz frequency divider counter reset. Clock function stops.

* After setting the RESET bit to "1", this bit is reset to "0" after a STOP condition is received, after restart, or after a 0.5s I²C-bus interface reset.

• TEST bit

The TEST bit is for manufacturer testing. Leave set to "0" for normal operation.

TEST	Description
0	Normal operating mode
1	Test mode

• RAM bit

Can be used as a general-purpose RAM bit.

• FIE (Frequency Interrupt Enable) bit

The FIE bit is the enable bit for the 50% duty, 1Hz signal output on INTN.

FIE	Description
0	INTN 1Hz output disable
1	INTN 1Hz output enable

* When power is applied, FIE is reset to "0" and INTN output disable is selected.

• TE (Timer Enable) bit

The TE bit enables the fixed-cycle timer down-counter.

TE	Counter operation
0	Timer count stop
1	Timer count start

* When power is applied, TE is reset to "0" and timer count stop is selected.

• TIE, AIE, UTIE (Timer, Alarm, Update Time Interrupt Enable) bits

The TIE, AIE, and UTIE bits enable the interrupt signal outputs on INTN. TIE controls the fixed-cycle timer interrupt output, AIE controls the alarm interrupt output, and UTIE controls the time update interrupt output.

TIE,AIE,UTIE	Description
0	INTN output disable
1	INTN output enable

* When power is applied, these bits are reset to "0" and INTN output disable is selected.

Revision History

DCO	REV	REVISION SUMMARY	PAGE	DATE
	-	Initial Release		05/30/2014
11540	A	Renamed P/N to QT2024L	ALL	06/08/15
		Update frequency stability vs. temperature codes	3	
10693	B	Correct Pinouts (Pins 1 - 3 incorrectly changed in Rev A)	2	10/09/2019