Revision Record							
Revision	**DCO**	**Description**	**Engineering Approval**	**Date**	**QA Approval**	**Date**	**Release Date**
-		Initial Release					
A		Modify tr/tf limits to better reflect output buffer drive capability.					2-27-07
B		Clarify temperature stability definitions, Table 1.					3-19-07
C		Modify microcircuit usage paragraph for clarification of microcircuit technology, SEL rating.					7-17-07
D		Change to microcircuit manufacturer.					8-8-08
E		Correction to Figure 1.					5-8-09
F		Update microcircuit usage paragraph. Update Table 3 and add notes to Figure 1.					
G	5573	Change document format/number. Update microcircuit usage. Update Table 1, code H. Add typical jitter to Table 3.	Curtis Hooper Richard Duong	05/25/16	Sipra Dasgupta	05/25/16	06/30/16
H	6571	Add Breadboard Model option Add par. 5.2.2, reference to F1221	Curtis Hooper Richard Duong	03/24/17 03/27/17	Daniel Moline	03/25/17	04/06/17
J	6837	Add EAR Destination Control Statement	Curtis Hooper Richard Duong	06/01/17 06/01/17	Daniel Moline	06/01/17	06/01/17
K	8974	Clarify Frequency digit count for marking purposes (Table 1)	Richard Duong Curtis Hooper	10/16/18 10/17/18	Daniel Moline	10/23/18	10/23/18
L	13495	Usage of AHC00: par. 6.4.3.1, Table 2	Richard Duong Curtis Hooper	05/10/21 05/10/21	Daniel Moline	05/14/21	05/17/21

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UNLESS OTHERWISE SPECIFIED Dimensions are in Inches Tolerances		
Decimal	**Fraction**	**Angular**
.xxx ± .005 .xx ± .02 .x ± .1	$^{x}/_{x} \pm {}^{1}/_{16}$	x° ± 2°

DETAIL PRODUCT SPECIFICATION CONTROL DRAWING

Initial Release	
Prepared	**Date**
Curtis Hooper	05/25/16
Checked	**Date**
Minh Dao	06/30/16
Engineering Approval	**Date**
Richard Duong	05/25/16
Quality Assurance Approval	**Date**
Sipra Dasgupta	05/25/16
Released	**Date**
Steven Nguyen	06/30/16

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TITLE

HYBRID CRYSTAL OSCILLATOR, CLASS S, QT625L, DETAIL SPECIFICATION FOR

DRAWING NO.			REVISION
QPDS-0118			**L**
SCALE	SIZE	CAGE CODE	PAGE
NONE	**A**	**51774**	**1** of **6**

1 PURPOSE

1.1 The purpose of this Detail Specification Control Drawing (SCD) is to describe the specific quality and reliability requirements for hybrid, hermetically sealed, crystal oscillators for use in space flight missions.

2 SCOPE

2.1 This specification establishes the minimum detail requirements for QT625L intended for use in conjunction with the applicable general SCD.

3 PART PROTECTION AND SAFETY

3.1 These items are susceptible to breakdown damage resulting from electrostatic discharge. Every precaution shall be taken while handling, installing, and testing the parts to prevent static charge. Care should be exercised to not apply more than rated voltage or current to any terminal/pad during testing.

4 PART NUMBER

4.1 The Q-Tech Part Number shall be as specified in Table 1 herein.

5 APPLICABLE DOCUMENTATION & REFERENCES

5.1 The following documents form a part of this drawing to the extent specified or modified herein.

5.2 **Q-Tech**

5.2.1 0401-00298-0001, Hybrid Crystal Oscillators, Class S, General Specification for

5.2.2 F1221, Definitions for Hybrid Product Development Levels

5.3 **Application of Documents**

5.3.1 **Issue of Documents**

Document revisions in effect on the date of the customer purchase order form a part of this drawing except as modified herein.

5.3.2 **Order of Precedence**

In the event of conflict between this document and the references cited herein or other requirements, the precedence in which requirements shall govern, in descending order, is as follows:

a) Applicable Customer Purchase Order
b) Applicable Q-Tech Corporation Detail SCD/Drawing
c) Applicable Q-Tech Corporation General SCD
d) Other Specifications, Standards, and Documentation Referenced Above

5.3.3 **Customer Purchase Order Special Requirements**

Additional special requirements shall be specified in the applicable customer purchase order when additional requirements or modifications are needed for compliance to special programs or product line compliance. Unique identification of the items produced may be required.

5.3.4 **General Specification Control Drawing**

Any reference to the “general specification” or “general SCD” refers to the Q-Tech Corporation General Specification Control Drawing cited in the Applicable Documentation and References section, unless otherwise specified.

6 GENERAL REQUIREMENTS

6.1 Definition of Requirements

Items supplied to this detail SCD shall meet the detail requirements specified herein.

6.2 Individual Item Requirements

The individual item requirements shall be in accordance with Q-Tech Corporation General SCD 0401-00298-0001 with the exceptions, modifications, and additions herein.

6.3 Approved Source of Supply

Hybrid crystal oscillators shall be supplied from the manufacturer specified in "Source of Supply" below.

6.4 Design and Construction

6.4.1 Outline Dimensions and Terminal Connections

The outline dimensions and terminal connections shall be as shown in Figure 1 herein.

6.4.2 Package Body and Lead Finish

The package body and lead finish shall be gold in accordance with MIL-PRF-38534.

6.4.3 Active Devices

The microcircuit used in this part shall use CMOS technology and shall be from a wafer proven to be radiation tolerant to 100 kRad (Si) total ionizing dose.

6.4.3.1 CMOS Microcircuit Usage

For frequencies below 3 MHz, the CMOS output microcircuit shall be 54AC191 (DLA SMD 5962-89749). For frequencies from 3 MHz but below 12MHz, the CMOS output microcircuit shall be 54AC74 (DLA SMD 5962-88520). For frequencies greater than or equal to 12 MHz and up to 70MHz, the CMOS microcircuit shall be 54AC00 (DLA SMD 5962-87549). These microcircuits are specified to be single event latch-up free for LET up to 93 MeV-cm^2/mg. For frequencies greater than 70 MHz, the CMOS microcircuit shall be 54AHC00 (DLA SMD 5962-18202). This microcircuit is specified to be single event latch-up free for LET up to 125 MeV-cm^2/mg.

6.5 Performance Requirements

6.5.1 Maximum Ratings

The maximum ratings shall be as specified in Table 2 herein.

6.5.2 Electrical Performance Characteristics and Limits

The electrical performance requirements and limits shall be in accordance with Table 3 herein.

6.5.3 Delta Limits

Except for frequency aging (refer to Table 3 herein), delta limits shall be in accordance with the general SCD.

6.5.4 Total Dose Radiation Limits

Hybrid crystal oscillators supplied in accordance with this detail SCD shall be capable of meeting the performance requirements after being exposed to 100 kRad (Si) total dose radiation levels.

7 QUALITY ASSURANCE PROVISIONS

7.1 General

The quality assurance provisions shall be in accordance with the general SCD with the exceptions, modifications, and additions specified herein.

7.2 Screening

The screening tests shall be in accordance with the general SCD.

7.3 **Quality Conformance Inspection (QCI)**

Quality Conformance Inspection shall be in accordance with the general SCD and shall be required only when specified by the purchase order.

8 PREPARATION FOR DELIVERY

8.1 **Preservation, Packaging, and Packing**

Hybrid crystal oscillators shall be prepared for delivery in accordance with the general SCD.

8.2 **Electrostatic Discharge Sensitivity**

The devices supplied to this detail SCD shall be considered to be electrostatic discharge sensitive and require further protection and shall use the packaging requirements class 1C in accordance with par. 3.9.5.8.2 of MIL-PRF-38534.

9 SOURCE OF SUPPLY

9.1 **Approved Manufacturer**

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6161 Chip Avenue
Cypress, CA 90630-5213 USA

10 NOTES

10.1 The notes of the general SCD are applicable to this drawing.

10.2 **Ordering Information**

The procuring activity shall advise Q-Tech Corporation at the time of Request for Quotation if quality conformance inspection is to be required.

Table 1 – Part Number

Model Number	Supply Voltage	Temperature Stability*	Screening	Frequency (MHz) (8 Digits)
QT625	L: 3.3	A: ±65 PPM, -55°C to +125°C	B: Breadboard Model	0.7500000 to 150.00000
		B: ±50 PPM, -55°C to +125°C	E: Engineering Model	
		C: ±50 PPM, -55°C to +105°C	M: Flight Model	
		D: ±40 PPM, -55°C to +105°C		
		E: ±30 PPM, -40°C to +85°C		
		F: ± 50 PPM, -20°C to +70°C		
		G: ±25 PPM, -20°C to +70°C		
		* H: ±5 PPM, 0°C to +55°C		

* Frequency/Temperature stability (tolerance) shall be referenced to the specified nominal output frequency, except for temp code H, in which case it is referenced to room temperature (T = 25 ± 2 °C). For temp code H, room temperature tolerance shall be ± 15 PPM.

Part Number Examples

QT625LBM-16.000000MHz would be a Flight Model QT625, CMOS, 3.3 Volts, stability ±50 PPM over -55°C to +125°C, @ 16MHz output.

QT625LEE-100.00000MHz would be an Engineering Model QT625, CMOS, 3.3 Volts, stability ±30 PPM over -40°C to +85°C, @ 100MHz output.

QT625LAB-120.00000MHz would be a Breadboard Model QT625, CMOS, 3.3 Volts, stability ±65 PPM over -55°C to +125°C, @ 120MHz output.

Table 2 – Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Units
Supply Voltage (≤70 MHz output)	V_{CC}	0	7	Volts
Supply Voltage (>70 MHz output)	V_{CC}	0	4.8	Volts
Operating Temperature	T_C	-55	+125	°C
Storage Temperature	T_{STG}	-65	+150	°C
Lead Solder Temperature/Time			+250/10	°C/Seconds
Package Thermal Resistance	Θ_{jc}		50	°C/W

Table 3 – Electrical Performance Characteristics

Electrical Parameter	Test Conditions (Note 2 and 3)	Limits				Notes
		Min.	Nom.	Max.	Units	
Frequency Range		0.75		150	MHz	
Frequency/Temperature Stability		See Table 1				Note 1, 4
Supply Voltage		2.97	3.3	3.63	Vdc	
Input Current Measured without load at 3.63 Vdc	**Output Frequency:**					
	Up to 59.99 MHz			15	mA	
	60 MHz – 99.99 MHz			20	mA	
	100 MHz – 150 MHz			30	mA	
Load			CMOS			Note 6
Output Voltage – Logic "0"				V_{cc} x 0.1	Vdc	
Output Voltage – Logic "1"		V_{cc} x 0.9			Vdc	
Output Waveform		Squarewave			N/A	
Rise / Fall Time	**Output Frequency:**					
	Up to 70 MHz			5	nsec	Note 7
	> 70 MHz – 125 MHz			3	nsec	Note 7
	> 125 MHz			2.5	nsec	Note 7
Duty Cycle		40	50	60	%	
Frequency Aging (After 30 Days)	70°C ± 3°C			±1.5	ppm	
Frequency Aging (After 1 Year)	70°C ± 3°C			±10	ppm	
Start Up Time				10	msec	
Jitter (cycle-to-cycle, rms)	**Output Frequency:**					
	Less than 3 MHz			40	ps	Note 8
	3 MHz – 150MHz			10	ps	Note 8

NOTES

1. The limit for Frequency Stability (tolerance) is referenced to the specified nominal output frequency, except for temp code H as noted above.
2. Unless otherwise specified, the limits are over the full operating temperature range, and under specified load conditions and nominal Supply Voltage.
3. Unless otherwise specified, all measurements are in accordance with MIL-PRF-55310.
4. Up to 30 days after shipment.
5. Voltage values are with respect to network ground terminal.
6. A standard CMOS load of 10 KΩ || 15 pF shall be used, except for frequencies greater than 125 MHz, where the load shall be 5 pF. See MIL-PRF-55310/26 for CMOS waveform measurement definitions.
7. Measured between 10% Vdc and 90% Vdc.
8. Guaranteed by design, not tested.

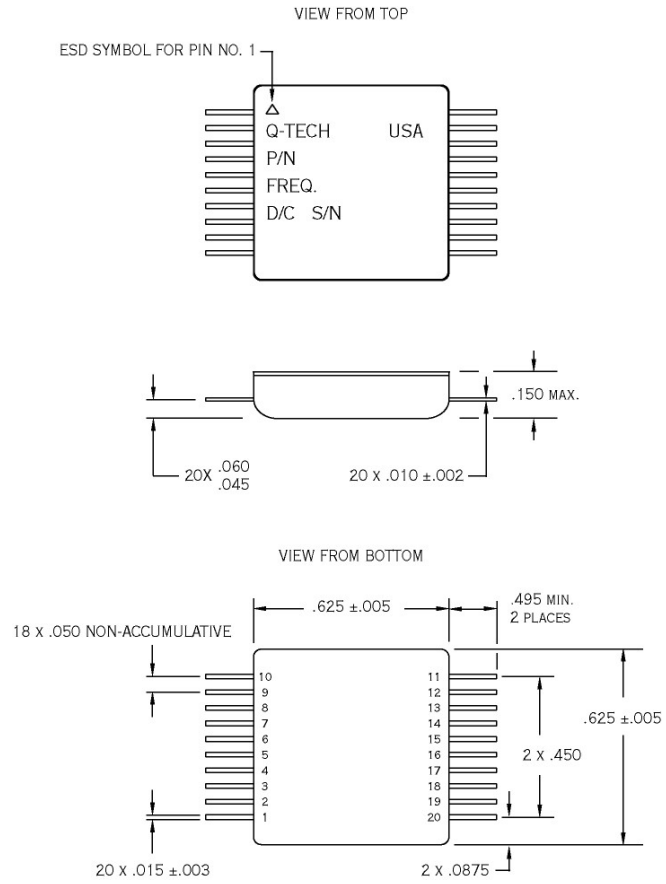

Figure 1 – Package Dimensions and Terminal Connections

Table 4 – Terminal Connections

Terminal No.	Connection	Terminal No.	Connection
1	N/C	11	OUTPUT
2	N/C	12	GROUND/CASE [4]
3	N/C	13	Vcc
4	N/C	14	N/C
5	N/C	15	GROUND/CASE [4]
6	N/C	16	N/C
7	N/C	17	N/C
8	N/C	18	N/C
9	N/C	19	N/C
10	GROUND/CASE	20	N/C

NOTES

1. Dimensions are in inches.
2. Lead numbers are for reference only and are not marked on the unit.
3. A triangle symbol is marked on the corner of the package to indicate Pin 1.
4. Additional Ground connections may be connected to circuit ground plane for minimum overshoot/ringing.