Q-TECH CORPORATION

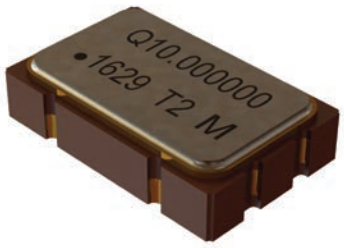
QT735 SERIES

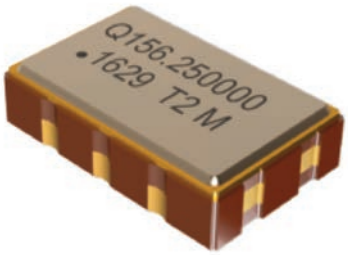
New Space Crystal Oscillator

3.2 x 5mm | 1.8V, 2.5V, 3.3V, 5Vdc | 1.000MHz to 250MHz

Description

Q-Tech's low profile extreme high shock hybrid oscillators consist of an IC operating at various supply voltages from 1.8V, 2.5V, 3.3V, and 5.0Vdc and a miniature strip quartz crystal. The series is offered in Surface-Mount SMT ceramic package. This is a small footprint package offered with a 50kRad(Si) TID for Low Earth Orbit (LEO) with high shock and high reliability space applications.





Features

- ECCN: EAR99
- 50kRad(Si) Total Dose Ionization
- Broad Frequency Range, 1.000MHz to 250MHz
- Small footprint, 3.2 x 5mm surface mount packages
- CMOS, LVDS, LVPECL
- Various Supply Voltages, 1.8Vdc to 5.0Vdc
- Wide Operating Temperature Range, -55°C to 125°C
- Tri-State Output
- Hermetically sealed package
- Fundamental and 3rd Overtone Designs
- Screening per MIL-PRF-55310, Level B, with PIND
- High Shock Resistant, tested up to 20,000g Mechanical Shock, Half-Sine, 0.3ms, All Axes
- Tape and Reel Packaging is available for an additional cost.
- Optional Hot Solder Dip, Sn60Pb40
- RoHS Compliant
- Note: Screening and test data is not serialized.

Applications

- Commercial satellites
- Low Earth Orbit
- New Space

Ordering Information

(Sample part number)

Q T 735 L D 10 M - 50.000MHz

Q	T	735	L	D	10	M	-	50.000MHz

Solder Dip Options
T = Standard
S = Sn60Pb40

Package (*)

Logic

AC	=	ACMOS	+5V (50pF)
HC	=	HCMOS	+5V (15pF)
LA	=	CMOS	+3.3V (50pF)
L	=	CMOS	+3.3V (15pF)
N	=	CMOS	+2.5V
R	=	CMOS	+1.8V
LW	=	LVDS	+3.3V
NW	=	LVDS	+2.5V
LP	=	LVPECL	+3.3V
NP	=	LVPECL	+2.5V

Tristate

D	=	Tristate on Pin 1
E	=	Tristate on Pin 2 (LVDS/LVPECL Only)

Temperature code (**)

6	=	±50ppm	at	-55°C to +105°C
9	=	±50ppm	at	-55°C to +125°C
10	=	±100ppm	at	-55°C to +125°C
11	=	±50ppm	at	-40°C to +85°C
12	=	±100ppm	at	-40°C to +85°C
15	=	±25ppm	at	-40°C to +85°C
16	=	±100ppm	at	-20°C to +70°C
17	=	±100ppm	at	-40°C to +125°C
20	=	±50ppm	at	-40°C to +125°C

Model/Screening
M = Screening per MIL-PRF-55310, Level B, modified
E = Engineering Model

Frequency
Output Frequency in MHz

(*) CMOS/TTL = 4 Pad, LVDS/LVPECL = 6 Pad

(**) Frequency stability vs. temperature codes may not be available in all frequencies. LVDS and LVPECL are only available with codes 11, 12, 15, or 16.

Parameters	QT735AC	QT735HC	QT735LA	QT735L	QT735N	QT735R
Output frequency range (Fo)	**1.544MHz — 75.000MHz**		**1MHz — 40MHz**	**32.768kHz, 1.000MHz — 125.000MHz**		**1.544MHz — 125.000MHz**
Supply voltage (Vdd)	5.0Vdc ± 10%		3.3Vdc ± 10%		2.5Vdc ± 10%	1.8Vdc ± 10%
Maximum Applied Voltage (Vdd max.)	-0.7 to +7.0Vdc		-0.5 to +5.0Vdc			-0.5 to +3.6Vdc
Frequency stability (ΔF/ΔT)	See Part Number on Page 1					
Operating temperature (Topr)	See Part Number on Page 1					
Storage temperature (Tsto)	-62ºC to + 125ºC					
Operating supply current (No Load)	10 mA max. - ≤ 20MHz 30 mA max. - 20MHz ~ ≤ 50MHz 40 mA max. - 50MHz ~ ≤ 75MHz		5 mA max. - <1.5MHz 7 mA max. - 1.5MHz ~ ≤ 20MHz 20 mA max. - 20MHz ~ ≤ 50MHz 30 mA max. - 50MHz ~ ≤ 100MHz 40 mA max. - 100MHz ~ 125MHz		5 mA max. - <1.5MHz 7 mA max. - 1.5MHz ~ ≤ 20MHz 15 mA max. - 20MHz ~ ≤ 50MHz 20 mA max. - 50MHz ~ ≤ 75MHz 25 mA max. - 75MHz ~ ≤ 100MHz 30 mA max. - 100MHz ~ 125MHz	5 mA max. - 1.5MHz ~ ≤ 20MHz 15 mA max. - 20MHz ~ ≤ 70MHz 20 mA max. - 70MHz ~ ≤ 100MHz 25 mA max. - 100MHz ~ 125MHz
Symmetry (50% of ouput waveform)	45/55%					
Rise and Fall times	8 ns max. - ≤ 20MHz 5 ns max. - 20MHz ~ ≤ 50MHz 2 ns max. - 50MHz ~ 75MHz 7 ns max. - **50pF Load** (20 ~ 40MHz)		200ns max. - 32.768kHz 6 ns max. - 1.000MHz ~ ≤ 20MHz 4 ns max. - 20MHz ~ ≤ 50MHz 3 ns max. - 50MHz ~ ≤ 75MHz 2 ns max. - 75MHz ~ 125MHz 7 ns max. - **50pF Load** (<40MHz)		200ns max. - 32.768kHz 6 ns max. - 1.000MHz ~ ≤ 20MHz 5 ns max. - 20MHz ~ ≤ 50MHz 3 ns max. - 50MHz ~ ≤ 75MHz 2 ns max. - 75MHz ~ 125MHz	6 ns max. - ≤ 20MHz 5 ns max. - 20MHz ~ ≤ 50MHz 3 ns max. - 50MHz ~ 125MHz
Output Load (Note 1)	50pF max.	15pF max.	50pF max.	15pF max.		
Start-up time (Tstup)	8ms max.					
Output voltage (Voh/Vol)	0.9Vdd min. / 0.1Vdd max.					
Output Current (Ioh/Iol)	± 16mA max.		± 8mA max.			
Enable/Disable function Pin 1	VIH ≥ 4.0V Active		VIH ≥ 2.0V Active		VIH ≥ 1.75V Active	VIH ≥ 1.26V Active
	VIL ≤ 0.8V High Z		VIL ≤ 0.5V High Z			
Phase Noise typ. @20.000MHz **(Note 2)**	10Hz -90 dBc/Hz 100Hz -124 dBc/Hz 1kHz -140 dBc/Hz 10kHz -148 dBc/Hz 100kHz -155 dBc/Hz 1MHz -157 dBc/Hz 10MHz -158 dBc/Hz					
Aging	±5ppm max. First Year ±2ppm max. Each Year Thereafter					

Note 1: 50pF Load is only available up to 50MHz
Note 2: Guaranteed by design, not tested.

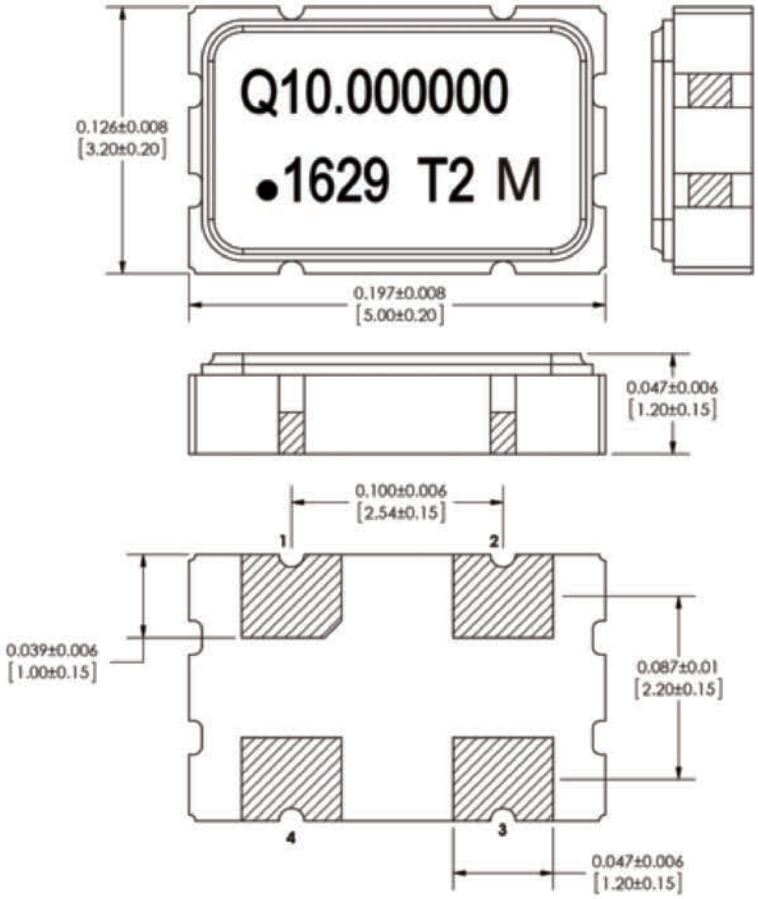
Electrical Performance Characteristics 25MHz to 250MHz LVDS

Parameters	QT735LP	QT735NP	QT735LW	QT735NW
Output frequency range (Fo)	**25.000MHz — 250.000MHz**		**80.000MHz — 250.000MHz**	
Supply voltage (Vdd)	3.3Vdc ± 5%	2.5Vdc ± 5%	3.3Vdc ± 5%	2.5Vdc ± 5%
Maximum Applied Voltage (Vdd max.)	-0.5 to +5.0Vdc		-0.5 to +5.0Vdc	
Logic	LVPECL		LVDS	
Frequency stability (ΔF/ΔT)	See Part Number on Page 1			
Operating temperature (Topr)	See Part Number on Page 1			
Storage temperature (Tsto)	-62ºC to + 125ºC			
Output Logic Levels Output Logic High (Voh) Output Logic Low (Vol)	 Vdd-1.025 < Voh < Vdd-0.880 Vdd-1.810 < Voh < Vdd-1.620		 Voh < 1.6 V Vol > 0.9 V	
Duty Cycle	45/55%			
Rise and Fall times	600ps typ. | 1000ps max.			
Load	50Ω into Vdd-2V		100Ω Differential	
Start-up time (Tstup)	10ms max.			
Current (No Load)	50mA typ. | 75mA max.		60mA max.	
Enable/Disable function (Pin 1 or Pin 2)	VIH ≥ 0.7*Vdd Active			
	VIL ≤ 0.3*Vdd High Z			
Phase Jitter (12kHz - 20MHz BW) **(Note 1)**	0.3ps nom. | 0.7ps max.		0.35ps nom. | 0.8ps max.	
Aging	±15ppm max over 10 years			

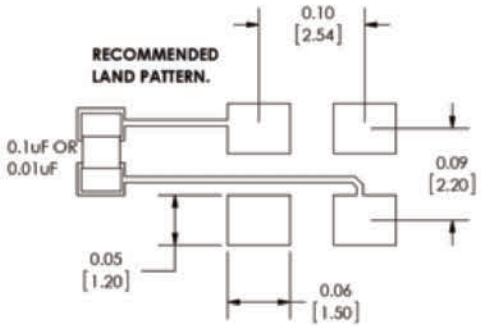
Notes:
1. Guaranteed by design, not tested.

Package Outline and Pin Connections (CMOS)

Dimensions are in inches (mm)



Pin No.	Function
1	TRISTATE
2	GND/CASE
3	OUTPUT
4	VDD



An external bypass capacitor 0.01µF is required between Vdd and GND

Marking

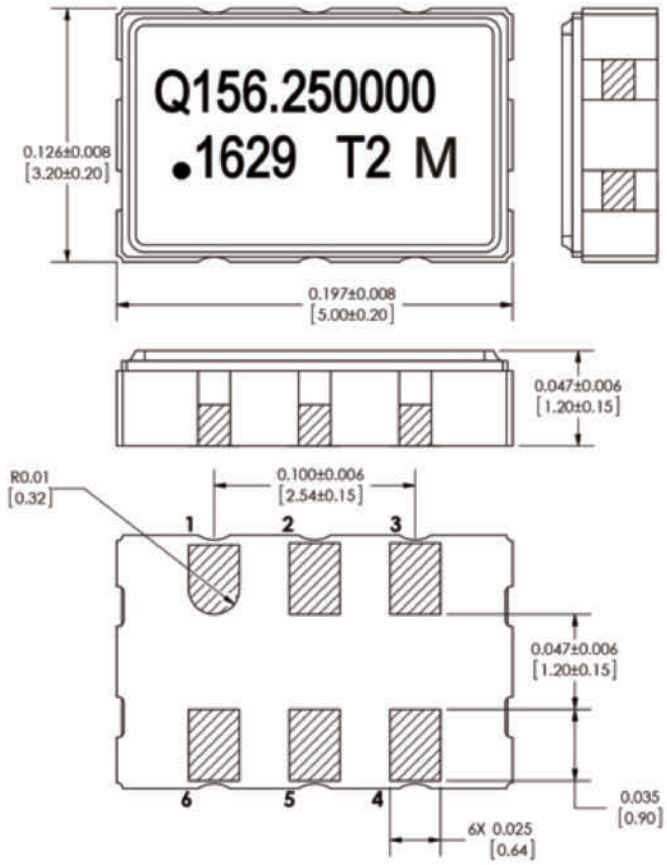
Line 1: QXXX.XXXXXX (Q for Q-Tech, no space 9 or 10 Characters of Frequency including decimal)
Line 2: Dot (Pin 1 Indicator), Date code (YY/WW), Internal Traceability Code, Part Level (M or E)

Package Information

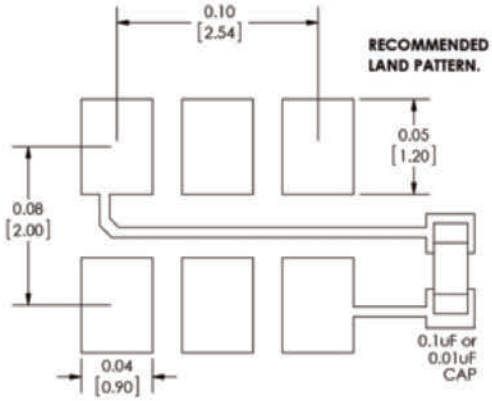
- Termination pads (4x), Electro nickel plating 1.27µm ~ 8.89µm typ., with gold 0.3µm ~ 1.0µm flash plate
- Weight: 0.057g typ.

Package Outline and Pin Connections (LVDS, LVPECL)

Dimensions are in inches (mm)



Pin No.	Function
1	ENABLE/DISABLE or NC
2	ENABLE/DISABLE or NC
3	GND/CASE
4	OUTPUT
5	COMP. OUTPUT
6	VDD



An external bypass capacitor 0.01µF is required between Vdd and GND

Marking

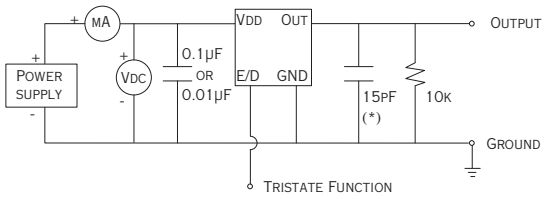
Line 1: QXXX.XXXXXX (Q for Q-Tech, no space 9 or 10 Characters of Frequency including decimal)
Line 2: Dot (Pin 1 Indicator), Date code (YY/WW), Internal Traceability Code, Part Level (M or E)

Package Information

- Termination pads (4x), Electro nickel plating 1.27µm ~ 8.89µm typ., with gold 0.3µm ~ 1.0µm flash plate
- Weight: 0.057g typ.

Test Circuit (CMOS)

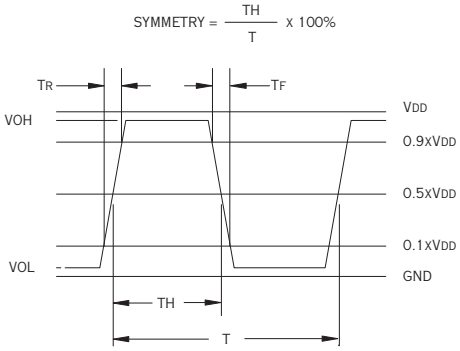
TYPICAL TEST CIRCUIT FOR CMOS LOGIC



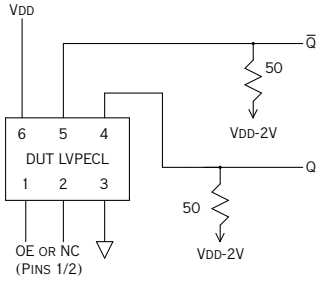
(*) CL INCLUDES PROBE AND JIG CAPACITANCE

The Tristate function on pin 1 has a built-in pull-up resistor so it can be left floating or tied to Vdd without deteriorating the electrical performance.

Output Waveform (CMOS, Typical)

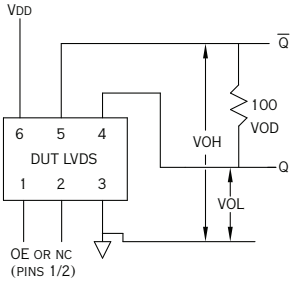


Test Circuit (LVPECL)



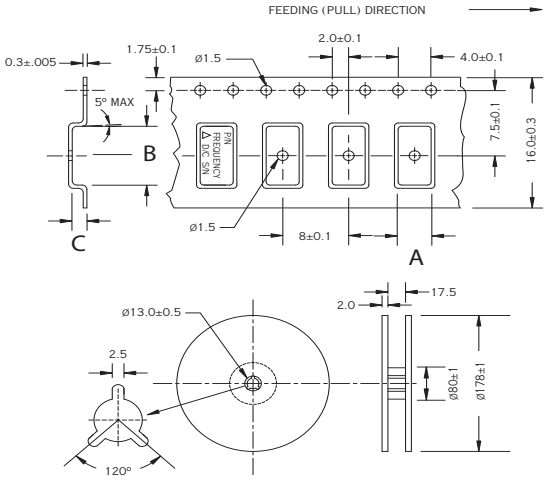
STANDARD TERMINATION LVPECL

Test Circuit (LVDS)



LVDS TERMINATION

Embossed Tape and Reel Information



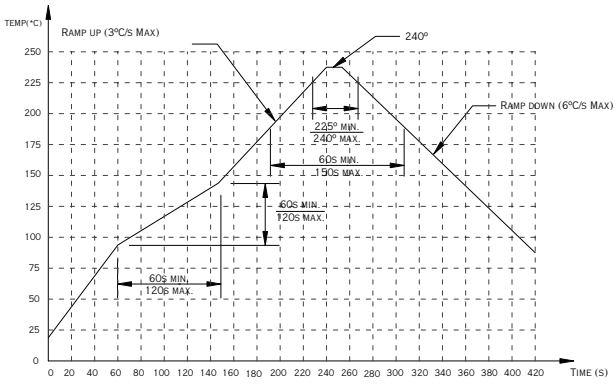
Dimensions are in mm. Tape is compliant to EIA-481-A.

Package	A	B	C
QT735	3.70 ±0.1	5.50 ±0.1	1.40 ±0.1

Reel size (Diameter in mm)	Qty per reel (pcs)
178	1,000

Reflow Profile

TYPICAL REFLOW PROFILE FOR SN-PB ASSEMBLY



SCREENING PER MIL-PRF-55310, LEVEL B PLUS PIND TEST

TEST	SPECIFICATION
Temperature Cycling	MIL-STD-883, Method 1010, Condition B
Constant Acceleration	MIL-STD-883, Method 2001, Test Condition A, Y1 axis only
Particle Impact Noise Detection	MIL-STD-883, Method 2020, Test Condition B
Fine Leak	MIL-STD-883, Method 1014, Condition A1 (See Note 1)
Gross Leak	MIL-STD-883, Method 1014, Condition C
Pre Burn-In	Electrical Test (Optional)
Burn-In (load)	Nominal Supply, +125°C for 160 hours minimum
Final Electrical Test	Electrical parameters test at +25°C only Frequency over specified operating temperature
External Visual	MIL-STD-883, Method 2009

NOTES:

1. Condition A1 Fine Leak Rate is $5x10^{-8}$ atm-cm^3/s Helium gas.

QUALITY CONFORMANCE INSPECTION TESTS (OPTIONAL)

GROUP	TEST METHOD	DESCRIPTION
A	MIL-PRF-55310, Level B, 100%	Electrical Tests (Supply voltage, Input Current, Output waveform, Rise and Fall times, Duty cycle, start-up time, overvoltage survivability, and 10 temperature frequency data points)
B	MIL-PRF-55310, Level B, 100%	Aging Test (Oscillator is energized in oven for a continuous period of 30 days at +70°C ± 3°C. The output frequency is measured within an interval of 72 hours maximum per MIL-PRF-55310)
C (Subgroups 1 to 4, excluding the “when specified” tests)	MIL-PRF-55310, Level B, sampling	4 (0)

ADDITIONAL INFORMATION

1) Design used a Class B integrated circuit, with Radiation hardness of 50kRad(Si) Total Ionizing Dose and a high Q cultured quartz.
2) ESD HBM Class 1C.
3) Standard packaging in anti-static plastic tube.
4) Screening and QCI data shall not be serialized.

DCO	REV	REVISION SUMMARY	PAGE	DATE
10402	-	Initial Release		09/11/2019
10717	A	Revise package and outline images to include product level code marking (M)	1, 4, 5	02/21/2020
		Update marking format for both packages (Line 2)	4, 5	
		Revise note (**) to remove unused temperature stability codes (5 and 18)	1	
		Add clarification to Rise and Fall time specification.	3	
		Remove jitter specifications that are not tested. Add notes to specifications that are not normally tested, but guaranteed by design.	2, 3	
		Fix Temp Stability code 16.	1	
11353	B	Remove Internal Visual and Stabilization Bake from screening table	7	03/11/2020
	C	Clarification of Screening final electrical tests	7	9/26/2025
		Separate LAD logic frequency range for clarification	2	