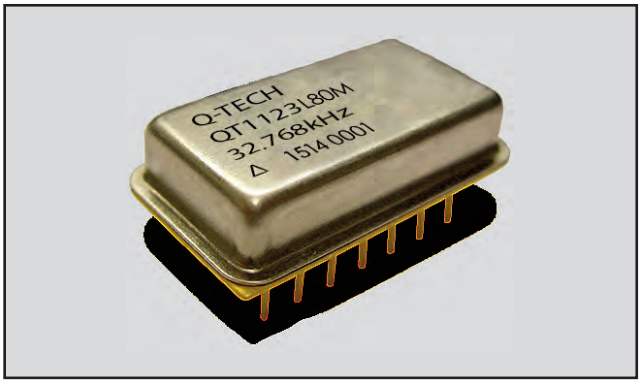
## Description

The QT1123 Real-Time Clock provides a time/calendar function, a 32 byte static RAM, and a 3 wire Serial Peripheral Interface (SPI Bus). The part is designed for high temperature applications with the on-board oscillator operating with a 32.768kHz output and the CMOS Serial Real-Time Clock. The time registers hold seconds, minutes, and hours, while the calendar registers hold day-of-week, date, month, and year information. The data is stored in BCD format. Other functions included alarm programmed to occur at a predetermined combination of seconds, minutes, and hours, the interrupt function, power fail detect with switching battery back-up power.




## Features

- Made in the USA
- ECCN: EAR99
- +3.3Vdc operation
- 32.768kHz square wave output
- Wide operating temperature (-55°C to +185°C)
- Very good stability
- Low current 90µA at +25°C
- SPI (Serial Peripheral Interface)
- Full Clock Features (Seconds, Minutes, Hours, Day, Week, Month, Year)
- 32 Wordx8 bit RAM
- Seconds, Minutes, Hours Alarm
- Automatic Power Loss Detection
- Low minimum Standby (Timekeeping) Voltage at 2.2V
- Buffered Clock Output
- Battery supply that powers oscillator and also connects to Vdd pin when power fails
- Three Independent Interrupt Modes
  - Alarm
  - Periodic
  - Power-Down Sense

## Electrical Parameters

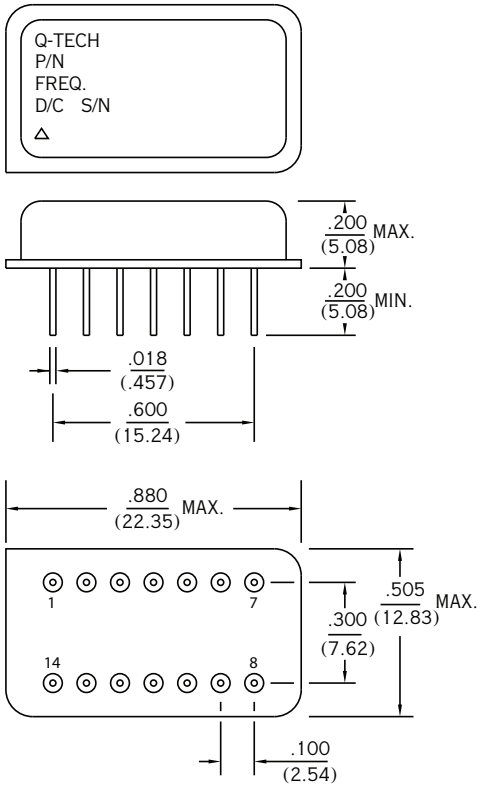
| Parameters | Rating |
|---|---|
| Output freq. (Fo) | **32.768kHz** |
| Supply voltage (Vdd) | 3.3Vdc ± 10% |
| Maximum Applied Voltage (Vdd max.) | +5Vdc |
| Freq. stability (ΔF/ΔT) | See Option codes |
| Operating temp. (Topr) | See Option codes |
| Storage temp. (Tsto) | -62ºC to + 150ºC |
| Operating supply current (Idd) (No Load) | 65µA Typ. at 25ºC<br>180µA max @185ºC, $V_{DD}$ = 3.3Vdc,25ºC<br>70µA max, $V_{BATT}$ = 2.3Vdc |
| Symmetry (50% of ouput waveform ) | 45/55% max. |
| Rise and Fall times (Tr/Tf) (with typical load) | 20 ns typ.<br>100 ns max.<br>(Measured from 10% to 90%) |
| Output Load | 15pF // 10kΩ |
| Start-up time (Tstup) | 10µs max. |
| Output voltage (Voh/Vol) | Voh = 2.4Vdc min.<br>Vol = 0.1 x Vdd max. |
| Output Current (Ioh/Iol) | ± 1mA min. |

## Applications

- Data logging
- Real Time Clock functions

## Package Outline and Pin Connections

### Dimensions are in inches (mm)




| Pin No. | Pin Name | Description |
|---|---|---|
| 1 | $\overline{CPUR}$ | CPU reset output pin. This pin functions as an N-Channel only, open-drain output and requires an external pull-up resistor. |
| 2 | CLK OUT | Clock output pin:The value in the three least significant bits of the Clock Control Register selects one of seven possible output frequencies to be used as the squarewave clock output:<br>0 = XTAL 4 = Disable (low output)<br>1 = XTAL/2 5 = 1Hz<br>2 = XTAL/4 6 = 2H<br>3 = XTAL/8 7 = 50Hz or 60Hz<br>XTAL Operation = 64Hz<br>All bits are reset by a power-on reset, therefore, the XTAL is selected as the clock output at this time. |
| 3 | SCK | Serial Clock Input:This input causes serial data to be latched from the MOSI input and shifted out on the MISO output |
| 4 | MOSI | Master Out/Slave In:Data bytes are shifted in at this pin, most significant bit (MSB) first.The Address/Control and Data bytes are shifted MSB first, Into the serial data input (MOSI) and out of the serial data output (MISO).Data is transferred into MOSI for a Write operation |
| 5 | MISO | Master In/Slave Out:Data bytes are shifted out at this pin, most significant bit (MSB) first.The Address/Control and Data bytes are shifted MSB first, Into the serial data input (MOSI) and out of the serial data output (MISO).Data is transferred out of MISO for a Read operation. |
| 6 | CE | Chip-enable input:A low level at this input holds the serial interface logic in a reset state, and disables the output driver at the MISO pin |
| 7 | GND | Ground pin : Connect this pin to ground |
| 8 | OUT | Oscillator Ouput Pin: Use this pin to monitor the internal Oscillator frequency and power |
| 9 | $V_{BATT}$ | The oscillator power source. The positive terminal of the battery should be connected to this pin. When the level on the $V_{SYS}$ pin falls below $V_{BATT}$ + 1.0V, the $V_{BATT}$ pin will be internally connected to the $V_{DD}$ ppin. |
| 10 | $\overline{INT}$ | Interrupt output pin:must be tied to an external pull-up resistor.The output is activated to a low level when:<br>1. Power-sense operation is selected (B5 = 1 in Interrupt Control Register) and a power failure occurs.<br>2. A previously set alarm time occurs. The alarm bit in the Status Register and interrupt-out signal are delayed 30.5µs when 32kHz operation is selected and 15.3µs for 2MHz and 7.6µs for 4MHz.<br>3. A previously selected periodic interrupt signal activates.The Status Register must be read to set the Interrupt output high after the selected periodic interval occurs. This is also true when conditions 1 and 2 activate the interrupt. If power-down had been previously selected, the interrupt will also reset the power-down functions."Interrupt True"- A high in this bit signifies that one of the three interrupts (Power Sense, Alarm, and Clock) is valid |
| 11 | $\overline{POR}$ | Power-on reset:A Schmitt-trigger input that generates a power-on internal reset signal using an external RC network.power-on-reset selects the device to be in the single supply or battery backup mode |
| 12 | NC | No connection |
| 13 | NC | No connection |
| 14 | VDD | The positive power-supply pin: Connect this pin to the power supply |

## Package Information

- Package material (header and leads): Kovar
- Lead finish: Gold Plated – 50µ ~ 80µ inches
  Nickel Underplate – 100µ ~ 250µ inches
- Package to lid attachment: Resistance weld
- Cover: Pure Nickel Grade A
- Weight: 3.4g typ.,14.2g max.

## Ordering Information

(Sample part number)

QT1123L80M-32.768kHz

**Q T 1123 L 80 M - 32.768kHz**

**Output Frequency**

**Solder Dip Option:**
T = Standard
S = Solder Dip (*)

**Screening Option:**
Blank = No Screening
M = Per MIL-PRF-55310, Level B

**Part Number**

**L=3.3Vdc**

**Operating Temperature Option:**

| | | | |
|---|---|---|---|
| 80 | = ±40ppm | @ 0ºC to +175ºC | (Operable up to + 185ºC) |
| 81 | = ±75ppm | @ 0ºC to +175ºC | (Operable up to + 185ºC) |
| 82 | = ±40ppm | @ -20ºC to +175ºC | (Operable up to + 185ºC) |
| 83 | = ±75ppm | @ -20ºC to +175ºC | (Operable up to + 185ºC) |
| 84 | = ±75ppm | @ 0ºC to +185ºC | |
| 85 | = ±75ppm | @ -20ºC to +185ºC | |
| 86 | = ±100ppm | @ -20ºC to +185ºC | |
| 87 | = ±150ppm | @ -20ºC to +185ºC | |
| 88 | = ±200ppm | @ -20ºC to +175ºC | (Operable up to + 185ºC) |
| 89 | = ±250ppm | @ -40ºC to +175ºC | (Operable up to + 185ºC) |
| 90 | = ±200ppm | @ -40ºC to +185ºC | |
| 91 | = ±250ppm | @ -40ºC to +185ºC | |
| 92 | = ±250ppm | @ -55ºC to +185ºC | |

**For Non-Standard requirements, contact Q-Tech Corporation at Sales@Q-Tech.com**

### Packaging Options

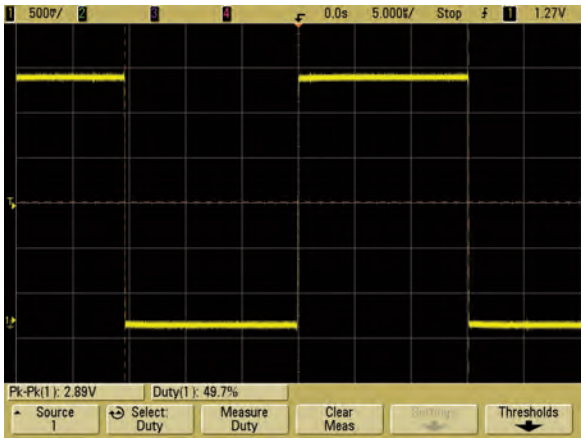
- Standard packaging in black foam
- Optional anti-static plastic tube

### Other Options Available For An Additional Charge

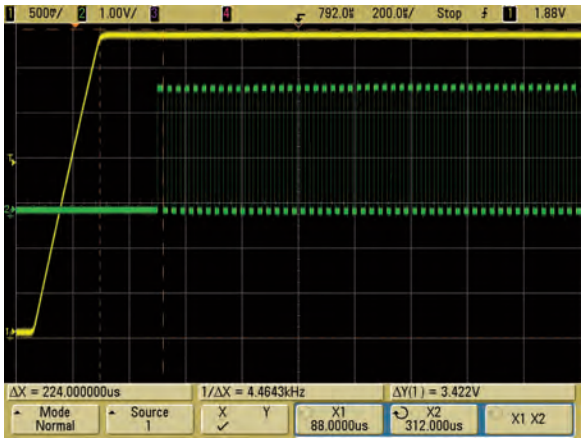
- Lead forming available. Please contact for details.
- Lead trimming
- P. I. N. D. test (MIL-STD 883, Method 2020)

(*) Hot Solder Dip options for an additional cost:
S = Sn60/Pb40 per MIL-PRF 55310

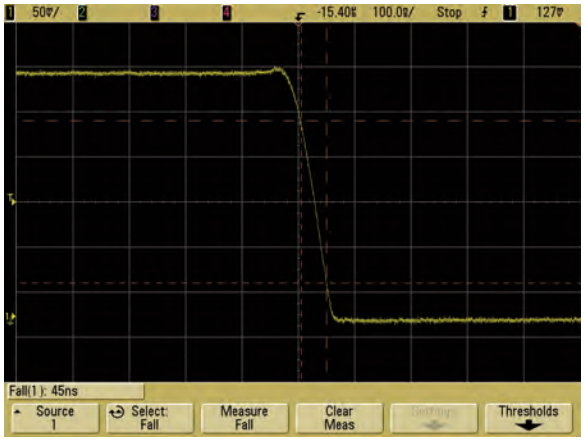
## Output Waveform (Typical)



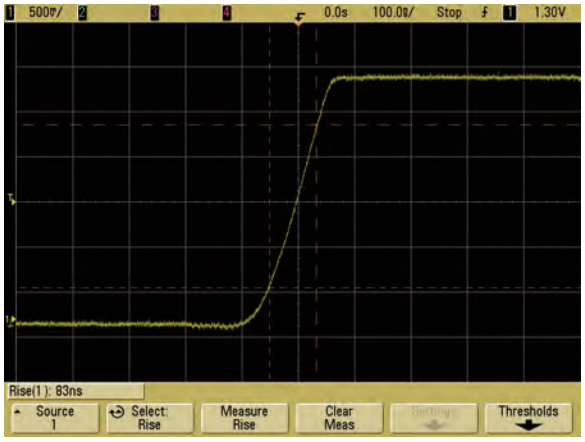

## Startup Time



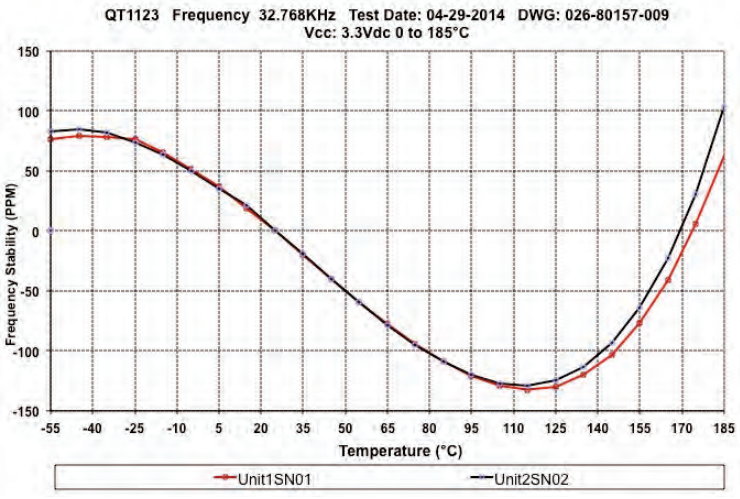

## Fall Time




## Rise Time

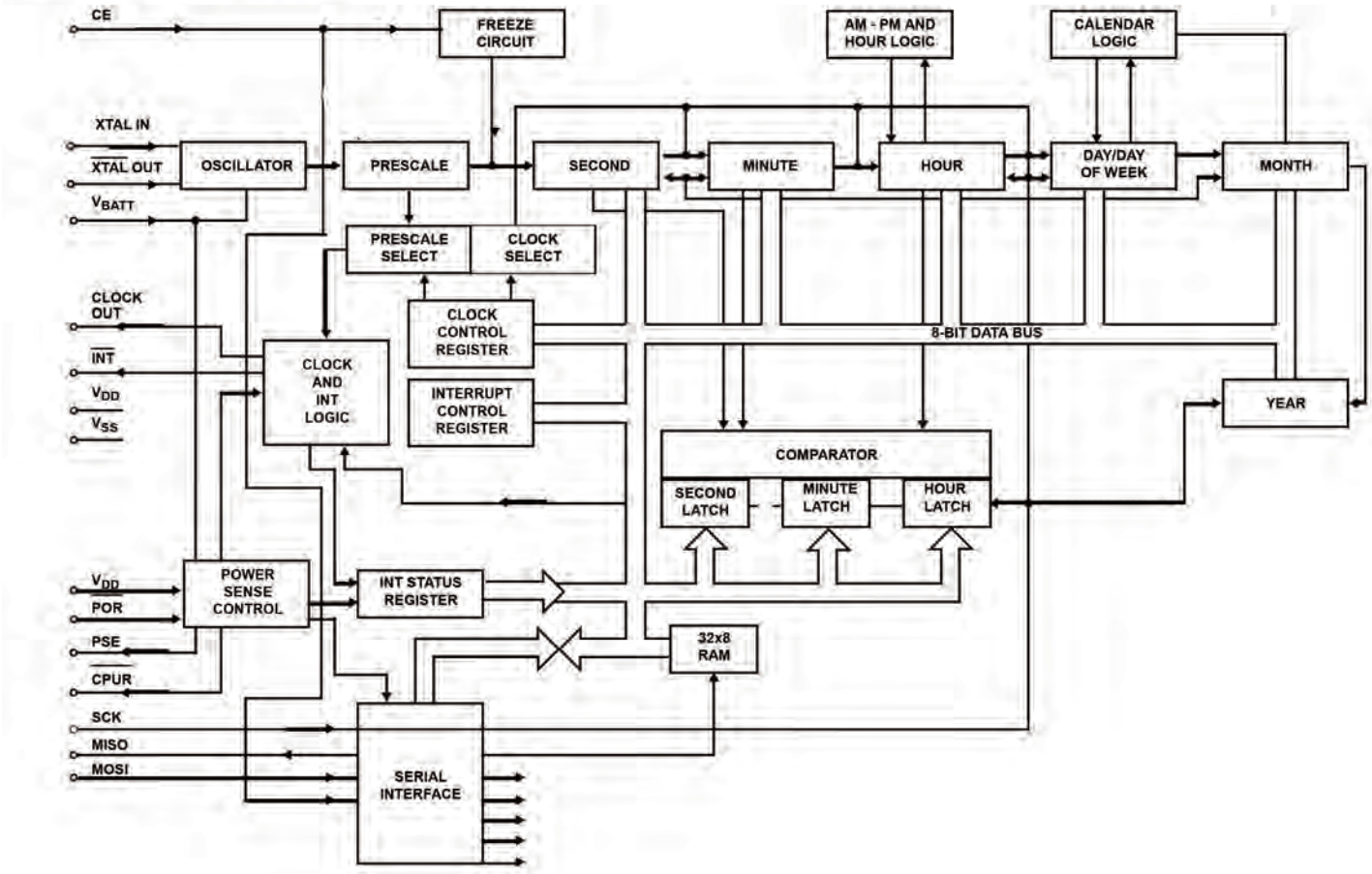



## Chart vs. Nominal



## QT1123 RTC Function Block

### Functional Block Diagram



## QT1123 Real Time Clock Programming Guide

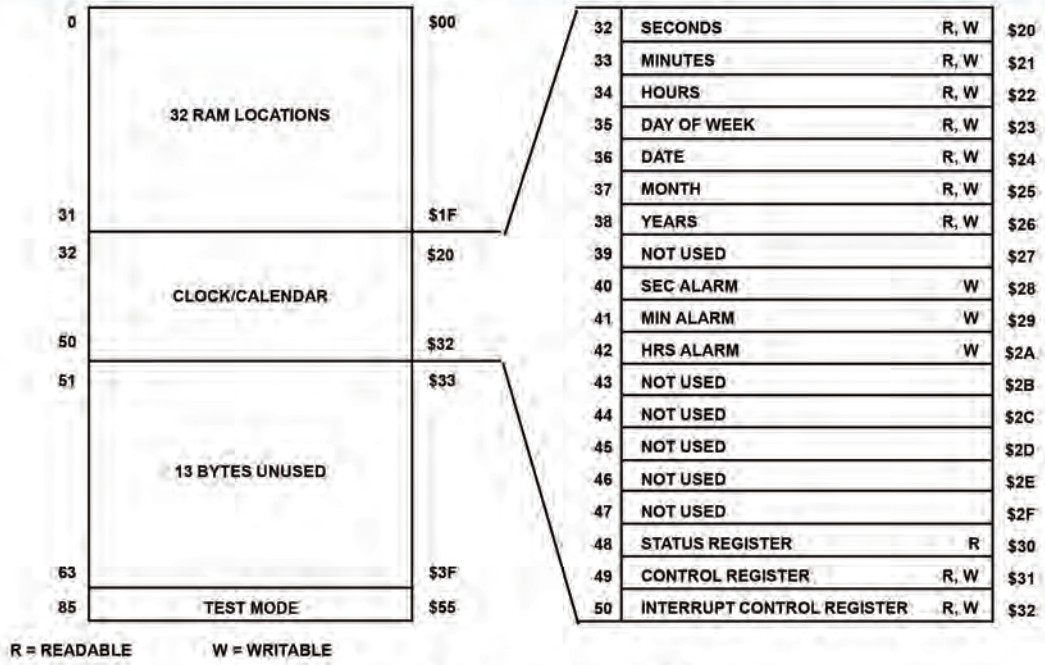



**FIGURE 1. ADDRESS MAP**

**TABLE 1. CLOCK/CALENDAR AND ALARM DATA MODES**

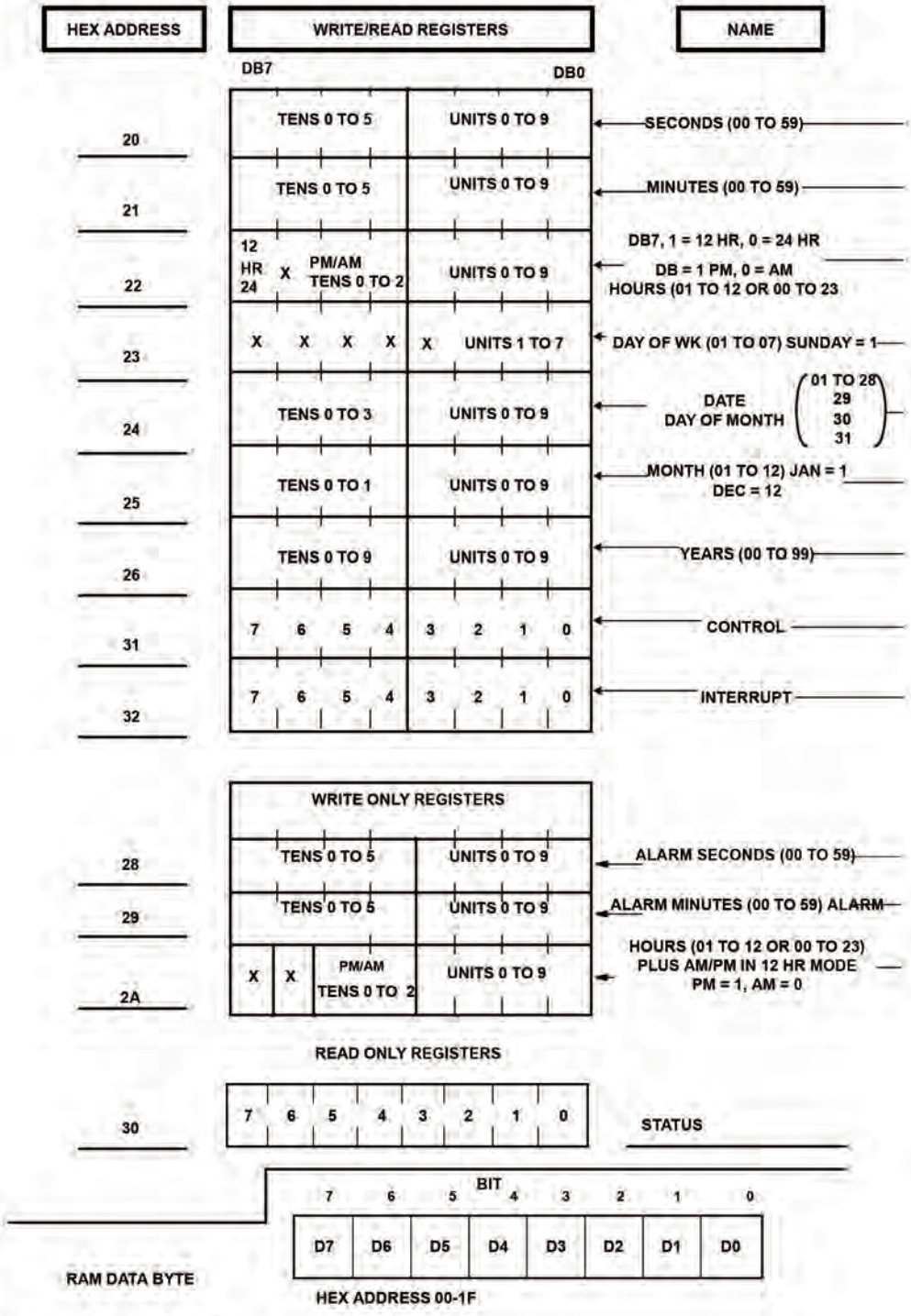
| ADDRESS LOCATION (H) | FUNCTION | DECIMAL RANGE | BCD DATA RANGE | BCD DATE EXAMPLE (Note 1) |
|---|---|---|---|---|
| 20 | Seconds | 0 to 59 | 00 to 59 | 18 |
| 21 | Minutes | 0 to 59 | 00 to 59 | 49 |
| 22 | Hours<br>12 Hour Mode<br>(Note 2) | 1 to 12 | 81 to 92 (AM)<br>A1 to B2 (PM) | A3 |
| | Hours<br>24 Hour Mode | 0 to 23 | 00 to 23 | 15 |
| 23 | Day of the Week<br>(Sunday = 1) | 1 to 7 | 01 to 07 | 03 |
| 24 | Day of the Month<br>(Date) | 1 to 31 | 01 to 31 | 29 |
| 25 | Month<br>Jan = 1, Dec = 12 | 1 to 12 | 01 to 12 | 10 |
| 26 | Years | 0 to 99 | 00 to 99 | 85 |
| 28 | Alarm Seconds | 0 to 59 | 00 to 59 | 18 |
| 29 | Alarm Minutes | 0 to 59 | 00 to 59 | 49 |
| 2A | Alarm Hours (Note 3)<br>12 Hour Mode | 1 to 12 | 01 to 12 (AM)<br>21 to 32 (PM) | 23 |
| | Alarm Hours<br>24 Hour Mode | 0 to 23 | 00 to 23 | 15 |

NOTES:

1. Example: 3:49:18, Tuesday. Oct. 29,1985.
2. Most significant Bit, D7, is "0" for 24 hours, and "1" for 12 hour mode. Data Bit D5 is "1" for PM and '0" for AM in 12 hour mode.
3. Alarm hours. Data Bit D5 is "1" for PM and "0" for AM in 12 hour mode. Data Bits D7 and D6 are DON'T CARE.

# QT1123 Real Time Clock Programming Guide

## Programmers Model - Clock Registers




NOTE: X = Don't care writes, X = 0 when read.

# QT1123 Real Time Clock Programming Guide

## Functional Description

The SPI real-time clock consists of a clock/calendar and a 32x8 RAM. Communications is established via the SPI (Serial Peripheral Interface) bus. In addition to the clock/calendar data from seconds to years, and system flexibility provided by the 32-byte RAM, the clock features computer handshaking with an interrupt output and a separate squarewave clock output that can be one of seven different frequencies. An alarm circuit is available that compares the alarm latches with the seconds, minutes and hours time counters and activates the interrupt output when they are equal. The clock is specifically designed to aid in power-down/power-up applications and offers several pins to aid the designer of battery backup systems.

### Mode Select

The voltage level that is present at the $V_{DD}$ input pin at the end of power-on-reset selects the device to be in the power supply or battery backup mode.

### Power Supply Mode

If $V_{DD}$ is a logic high when power-on-reset is completed, CLK OUT, PSE and CPUR will be enabled and the device will be completely operational. CPUR will be placed low if the logic level at the $V_{DD}$ pin goes low. If the output signals CLK OUT, PSE and CPUR are disabled due to a power-down instruction, $V_{DD}$ brought to a logic low and then to a logic high will re- enable these outputs.

### Battery Backup Mode

If $V_{DD}$ is a logic low at the end of power-on-reset, the device is in the battery backup mode. When $V_{DD}$ is brought to a logic high, the device will switch to power supply mode.

### Clock/Calendar (See Figure 1)

The clock/calendar portion of this device consists of a long string of counters that is toggled by a 1Hz input. The 1Hz input is generated by a prescaler driven by an on-board oscillator that utilizes one of four possible external crystals or that can be driven by an external clock source.

The time counters offer seconds, minutes and hours data in 12 hour or 24 hour format. An AM/PM indicator is available that once set, toggles every 12 hours. The calendar counters consist of day (day of week), date (day of month), month and years information. Data in the counters is in BCD format. The hours counter utilizes BCD for hour data plus bits for 12/24 hour and AM/PM. The seven time counters are accessed serially at addresses 20H through 26H. See Table 1.

### RAM

The real-time clock also has a static 32x8 RAM that is located at addresses 00-1FH. Transmitting the address/control word with Bit 5 low selects RAM access. Bits 0 through 4 select the RAM location.

### Alarm

The alarm is set by accessing the three alarm latches and loading the required data. The alarm latches consist of seconds, minutes and hours registers. When their outputs equal the values in the seconds, minutes and hours time counters, an interrupt is generated. The interrupt output will go low if the alarm bit in the Interrupt Control Register is set high. The alarm interrupt bit in the Status Register is set when the interrupt occurs. To preclude a false interrupt when loading the time counters, the alarm interrupt bit should be set low in the Interrupt Control Register. This procedure is not required when the alarm time is set.

### Watchdog Function

When Bit 7 in the Interrupt Control Register is set high, the Clock's CE (chip enable) pin must be toggled at a regular interval without a serial data transfer. If the CE is not toggled, the clock will supply a CPU reset pulse and Bit 6 in the Status Register will be set.

### Clock Out

The value in the three least significant bits of the Clock Control Register selects one of seven possible output frequencies. This squarewave signal is available at the CLK OUT pin. When power-down operation is initiated, the output is set low.

### Control Registers and Status Registers

The operation of the Real-Time Clock is controlled by the Clock Control and Interrupt Control Registers. Both registers are Read-Write Registers. Another register, the Status Register, is available to indicate the operating conditions. The Status Register is a Read only Register.

# QT1123 Real Time Clock Programming Guide

## Clock Control Register

**CLOCK CONTROL REGISTER (Write/Read) - Address 31H**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| START | X | XTAL | XTAL | X | CLK OUT | CLK OUT | CLK OUT |
| | | SEL | SEL | | | | |
| $\overline{\text{STOP}}$ | $\overline{\text{XTAL}}$ | 1 | 0 | $\overline{\text{X}}$ | 2 | 1 | 0 |

### Start-Stop

A high written into this bit will enable the counter stages of the clock circuitry. A low will hold all bits reset in the divider chain from 32Hz to 1Hz. A clock out selected by Bit 0, Bit 1 and Bit 2 will not be affected by the stop function except the 1Hz and 2Hz outputs.

### XTAL

When the bit is low, the crystal input will generate the 1Hz time update. This bit should be low all the time for QT1123.

### XTAL Select

One of 4 possible crystals is selected by value in these two bits:

0 = 4.194304MHz 2 = 1.048576MHz

1 = 2.097152MHz 3 = 32,768Hz

For QT1123, always select 3 (i.e. xtal frequency=32.768kHz)

### Clock Out

The three bits specify one of the 7 frequencies to be used as the squarewave clock output:

0 = XTAL 4 = Disable (low output)
1 = XTAL/2 5 = 1Hz
2 = XTAL/4 6 = 2Hz
3 = XTAL/8 7 = Do not care

All bits are reset by a power-on reset. Therefore, the XTAL is selected as the clock output at this time.

## Interrupt Control Register

**INTERRUPT CONTROL REGISTER (Write/Read) - Address 32H**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| WATCHDOG | POWER DOWN | Do not care | ALARM | PERIODIC SELECT | | | |

NOTE: All bits are reset by power-on reset.

### Watchdog

When this bit is set high, the watchdog operation will be enabled. This function requires the CPU to toggle the CE pin periodically without a serial-transfer requirement. In the event this does not occur, a CPU reset will be issued. Status Register must be read before re-enabling watchdog.

### Power-Down

A high in this location will initiate a power down. A CPU reset will occur, the CLK OUT and PSE output pins will be set low and the serial interface will be disabled.

### Alarm

The output of the alarm comparator is enabled when this bit is set high. When a comparison occurs between the seconds, minutes and hours time and alarm counters, the interrupt output is activated. When loading the time counters, this bit should be set low to avoid a false interrupt. This is not required when loading the alarm counters.

# QT1123 Real Time Clock Programming Guide

***Periodic Select***

The value in these 4 bits will select the frequency of the periodic output. (See Table 3).

**TABLE 3. PERIODIC INTERRUPT OUTPUT**

| D0 - D3 VALUE | PERIODIC INTERRUPT OUTPUT FREQUENCY | XTAL |
|---|---|---|
| 0 | Disable | |
| 1 | 2048Hz | X |
| 2 | 1024Hz | X |
| 3 | 512Hz | X |
| 4 | 256Hz | X |
| 5 | 128Hz | X |
| 6 | 64Hz | X |
| 7 | 32Hz | X |
| 8 | 16Hz | X |
| 9 | 8Hz | X |
| 10 | 4Hz | X |
| 11 | 2Hz | X |
| 12 | 1Hz | X |
| 13 | Minute | X |
| 14 | Hour | X |
| 15 | Day | X |

# QT1123 Real Time Clock Programming Guide

## Status Register

**STATUS REGISTER (Read Only) - Address 30H**

| D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|
| X | WATCHDOG | TEST MODE | FIRST TIME UP | INTERRUPT TRUE | X | ALARM INTERRUPT | CLOCK INTERRUPT |

**TRUTH TABLE**

| MODE | SIGNAL | | | |
|---|---|---|---|---|
| | CE | SCK (Note 4) | MOSI | MISO |
| DISABLE RESET | L | INPUT DISABLED | INPUT DISABLED | HIGH Z |
| WRITE | H | CPOL = 1  CPOL = 0 | DATA BIT LATCH | HIGH Z |
| READ | H | CPOL = 1  CPOL = 0 | X | NEXT DATA BIT SHIFTED OUT (Note 5) |

NOTES:

4. When interfacing to microcontrollers, serial clock phase bit, CPHA, must be set = 1 in the microcomputer's Control Register.
5. MISO remains at a high Z until 8-bits of data are ready to be shifted out during a READ. It remains at a high Z during the entire WRITE cycle.

### Watchdog

If this bit is set high, the watchdog circuit has detected a CPU failure.

### Test Mode

When this bit is set high, the device is in the TEST MODE.

### First-time Up

Power-on reset sets this bit high. This signifies that data in the RAM and Clock is not valid and should be initialized.

### Interrupt True

A high in this bit signifies that one of the two interrupts (Alarm and Clock) is valid.

### Alarm Interrupt

When the seconds, minutes and hours time and alarm counter are equal, this bit will be set high. Status Register must be read before loading Interrupt Control Register for valid alarm indication after alarm activates.

### Clock Interrupt

A periodic interrupt will set this bit high.

All bits are reset by a power-on reset except the "FIRST- TIME UP" which is set. All bits except the power-sense bit are reset after a read of this register.

# QT1123 Real Time Clock Programming Guide

## SPI Interface Pin Signal Description

### SCK (Serial Clock Input) (Note6)

This input causes serial data to be latched from the MOSI input and shifted out on the MISO output.

### MOSI (Master Out/Slave In) (Note6)

Data bytes are shifted in at this pin, most significant bit (MSB) first.

### MISO (Master In/Slave Out)

Data bytes are shifted out at this pin, most significant bit (MSB) first.

### CE (Chip Enable) (Note7)

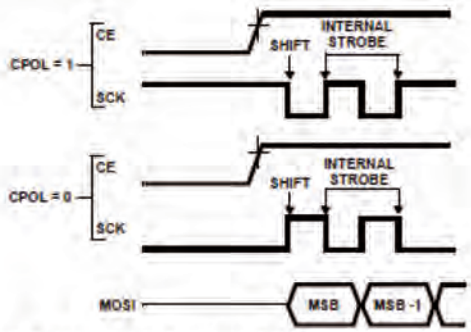
A positive chip-enable input. A low level at this input holds the serial interface logic in a reset state, and disables the output driver at the MISO pin.

NOTES:

6. These inputs will retain their previous state if the line driving them goes into a High-Z state.
7. The CE input has as internal pull-down device, if the input is in a low state before going to High Z, the input can be left in a High Z.

## Functional Description

The Serial Peripheral Interface (SPI) utilized by the QT1123 is a serial synchronous bus for address and data transfers. The clock, which is generated by the microcomputer is active only during address and data transfers. A unique feature of the QT1123 is that it automatically determines the level of the inactive clock by sampling SCK when CE becomes active (see Figure 8). Input data (MOSI) is latched internally on the internal strobe edge and output data (MISO) is shifted out on the shift edge, as defined by Figure 8. There is one clock for each data bit transferred (address, as well as data bits are transferred in groups of 8).




NOTE: "CPOL" is a bit that is set in the microcomputer's Control Register.

FIGURE 8. SERIAL RAM CLOCK (SCK) AS A FUNCTION OF MCU CLOCK POLARITY (CPOL)

## Address and Data Format

There are three types of serial transfer:

1. Address Control - Figure 9.
2. READ or WRITE Data - Figure 10.
3. Watchdog Reset (actually a non-transfer) Figure 11.

The Address/Control and Data bytes are shifted MSB first, into the serial data input (MOSI) and out of the serial data output (MISO).

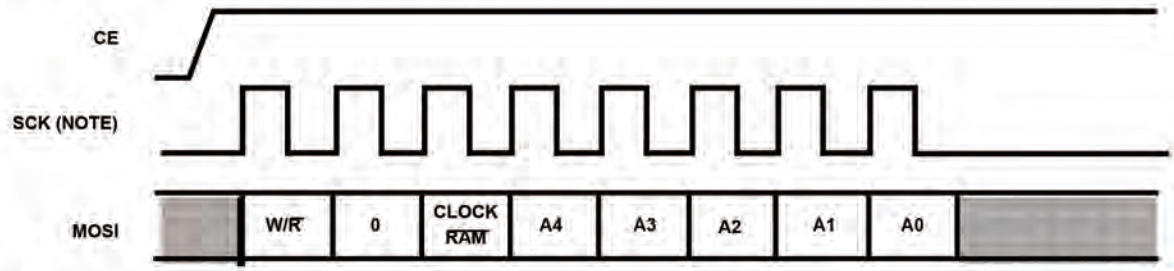
Any transfer of data requires an Address/Control byte to specify a Write or Read operation and to select a Clock or RAM location, followed by one or more bytes of data.

Data is transferred out of MISO for a Read and into MOSI for a Write operation.

# QT1123 Real Time Clock Programming Guide

***Address/Control Byte - (see Figure 9)***

It is always the first byte received after CE goes true. To transmit a new address, CE must first go false and then true again. Bit 5 is used to select between Clock and RAM locations

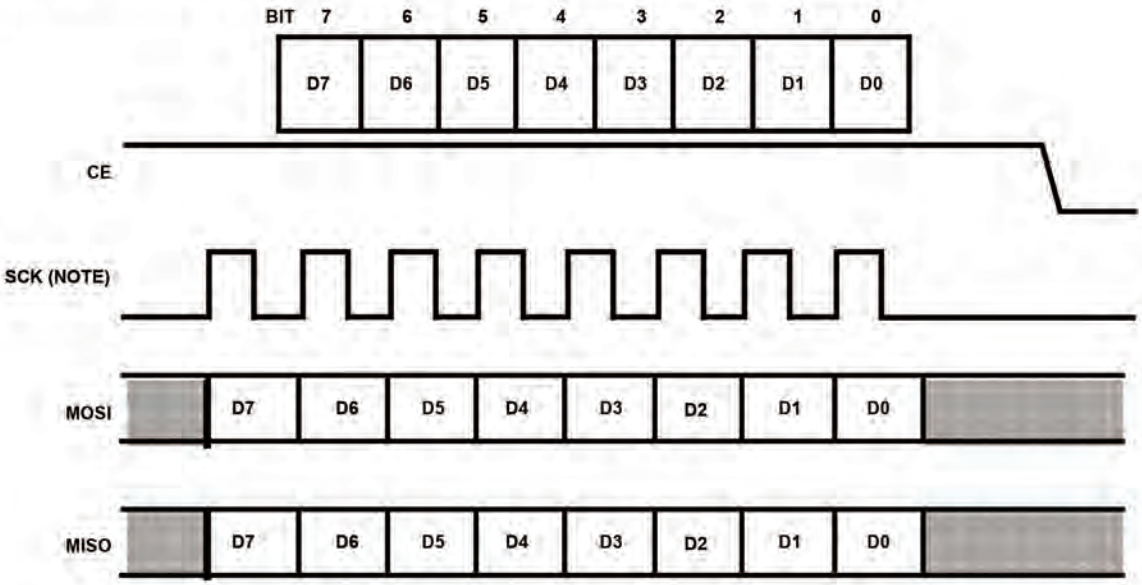



NOTE: SCK can be either polarity.

**FIGURE 9. ADDRESS/CONTROL BYTE-TRANSFER WAVEFORMS**

***Read/Write Data* (See Figure 10)**

Read/Write data follows the Address/Control byte.




NOTE: SCK can be either polarity.

**FIGURE 10. READ/WRITE DATA TRANSFER WAVEFORMS**

# QT1123 Real Time Clock Programming Guide

### *Watchdog Reset* (See Figure 11)

When watchdog operation is selected, CE must be toggled periodically or a CPU reset will be outputted.

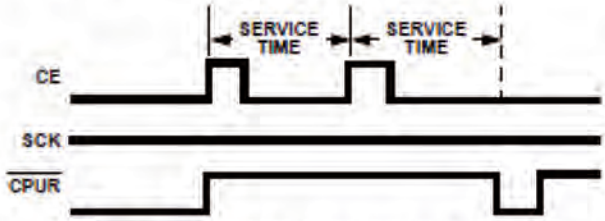



FIGURE 11. WATCHDOG OPERATION WAVEFORMS

### *Address and Data*

Data transfers can occur one byte at a time (Figure 12) or in a multibyte burst mode (Figure 13). After the Real-Time Clock enabled, an Address/Control word is sent to set the CLOCK or RAM and select the type of operation (i.e., Read or Write). For a single-byte Read or Write, one byte is transferred to or from the Clock Register or RAM location specified in the Address/Control byte and the Real-Time Clock is then disabled. Write cycle causes the latched Clock Register or RAM address to automatically increment. Incrementing continues after each transfer until the device is disabled. After incrementing to 1FH the address will "wrap" to 00H and continue. Therefore, when the RAM is selected the address will "wrap" to 00H and when the clock is selected the address will "wrap" 20H.

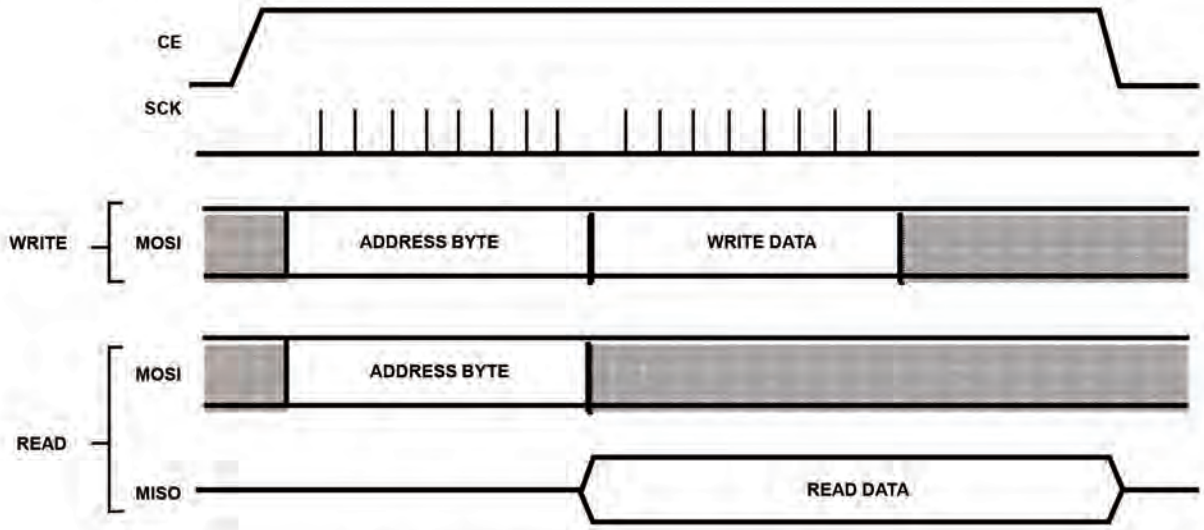



FIGURE 12. SINGLE-BYTE TRANSFER WAVEFORMS

## QT1123 Real Time Clock Programming Guide

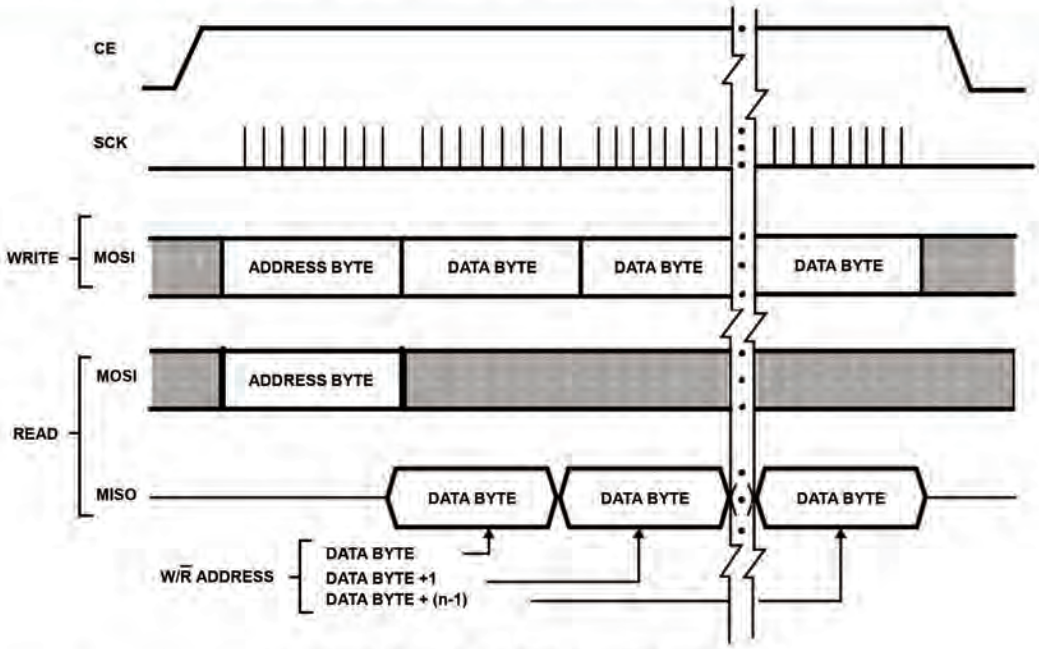



FIGURE 13. MULTIPLE-BYTE TRANSFER WAVEFORMS

### *Timing Diagrams*

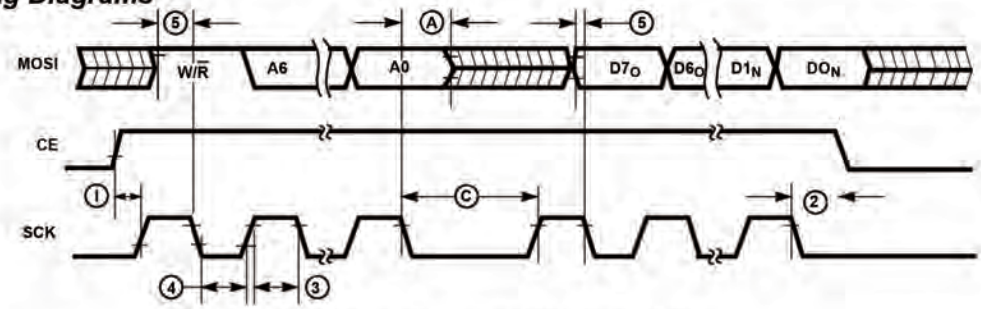



FIGURE 14. WRITE-CYCLE TIMING WAVEFORMS

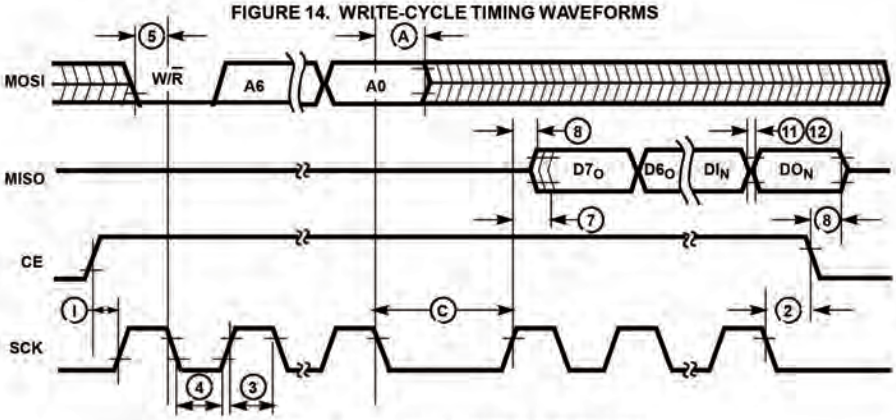
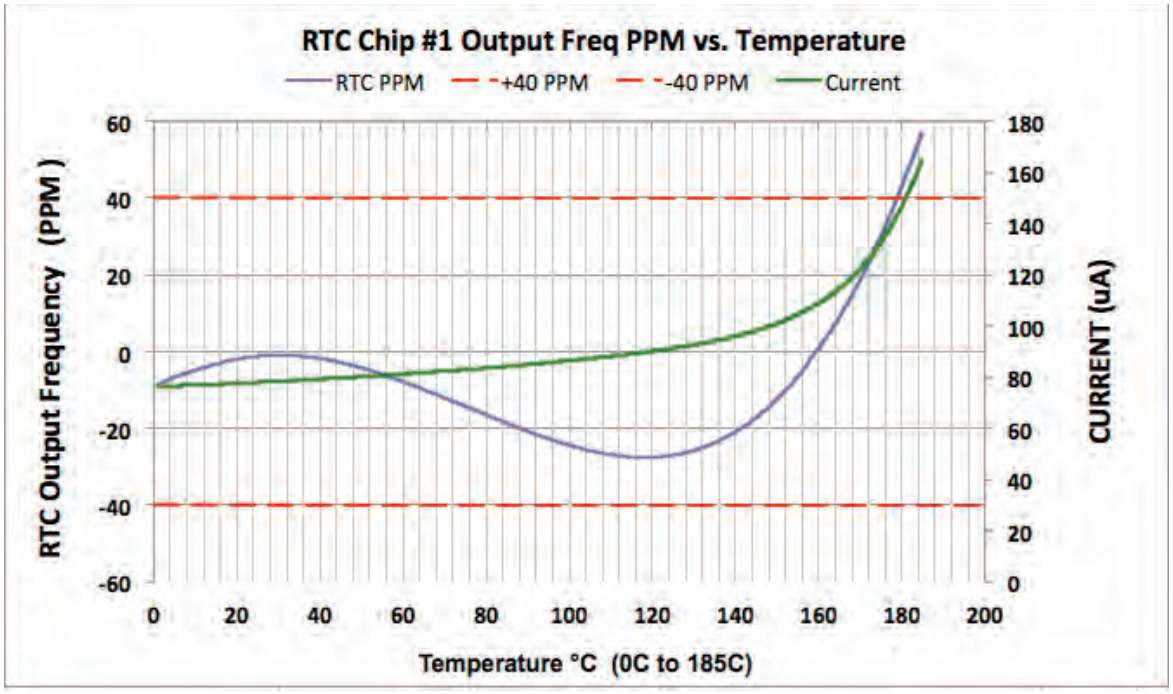


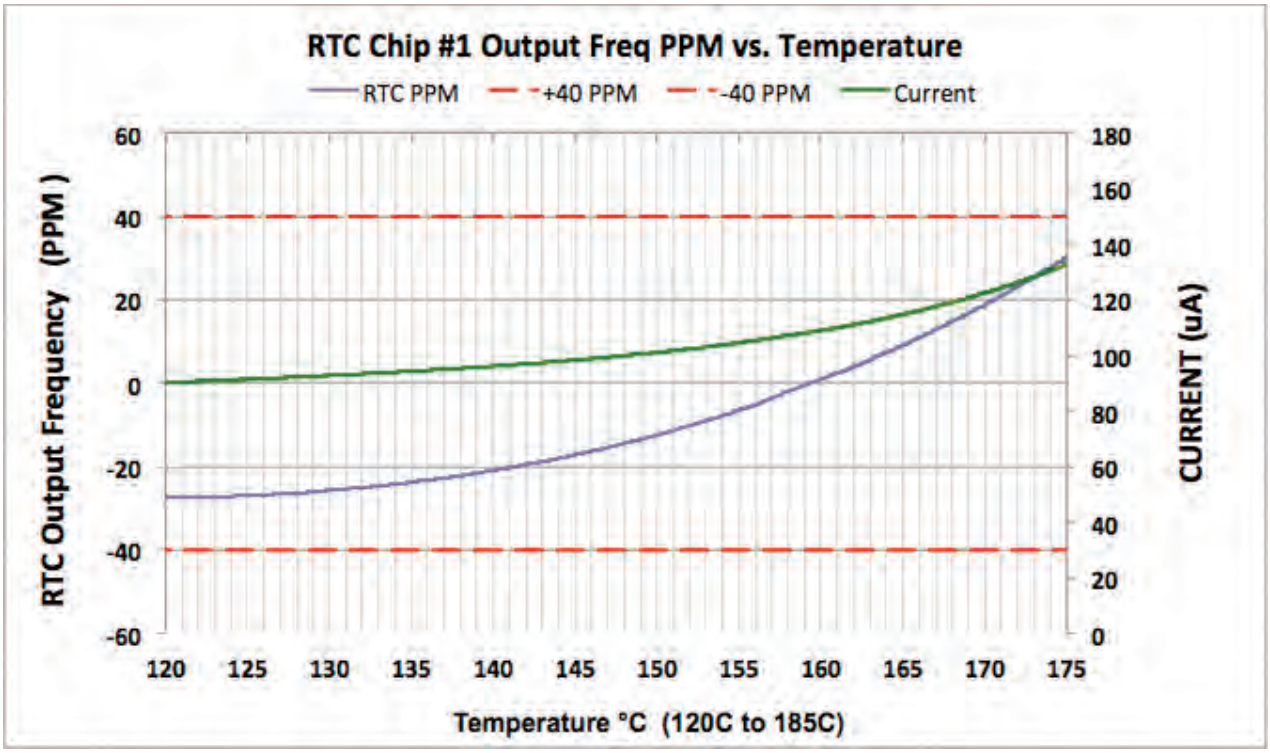

FIGURE 15. READ-CYCLE TIMING WAVEFORM

11

| | |
|---|---|
| DESCRIPTION: RTC CHIP #1 with LOW Current OSC | TEST DATE: 5/27/15 |
| PART NO: N/A | TEST PHASE: Eng Eval 0C TO 185C |
| SERIAL NUMBER #: RTC CHIP #1 | OPERATOR: D.Goderich |

| CURRENT TIME | RTC OUTPUT FREQ BEFORE FINAL ADJUSTED | PPM Delta from (25C) | SYS I (uA) | Temperature (°C) |
|---|---|---|---|---|
| Wed 27/May/2015 10:50:05 AM | 32822.4648 | -8.6 | 76.38 | 0.80 |
| Wed 27/May/2015 10:50:06 AM | 32822.4648 | -8.6 | 76.31 | 0.80 |
| Wed 27/May/2015 10:50:08 AM | 32822.4648 | -8.6 | 76.34 | 0.80 |
| Wed 27/May/2015 10:50:10 AM | 32822.4648 | -8.6 | 76.35 | 0.80 |
| Wed 27/May/2015 10:50:11 AM | 32822.4648 | -8.6 | 76.30 | 0.80 |
| Wed 27/May/2015 10:50:12 AM | 32822.4648 | -8.6 | 76.27 | 0.80 |
| Wed 27/May/2015 10:50:13 AM | 32822.4609 | -8.7 | 76.35 | 0.80 |
| Wed 27/May/2015 10:50:14 AM | 32822.4648 | -8.6 | 76.40 | 0.80 |
| Wed 27/May/2015 10:50:16 AM | 32822.4609 | -8.7 | 76.37 | 0.80 |
| Wed 27/May/2015 10:50:18 AM | 32822.4609 | -8.7 | 76.36 | 0.80 |
| Wed 27/May/2015 10:50:19 AM | 32822.4609 | -8.7 | 76.34 | 0.80 |
| Wed 27/May/2015 10:50:20 AM | 32822.4609 | -8.7 | 76.38 | 0.80 |
| Wed 27/May/2015 10:50:22 AM | 32822.4609 | -8.7 | 76.34 | 0.80 |
| Wed 27/May/2015 10:50:24 AM | 32822.4609 | -8.7 | 76.35 | 0.80 |
| Wed 27/May/2015 10:50:25 AM | 32822.4609 | -8.7 | 76.34 | 0.80 |
| Wed 27/May/2015 10:50:26 AM | 32822.4609 | -8.7 | 76.33 | 0.80 |
| Wed 27/May/2015 10:50:28 AM | 32822.4609 | -8.7 | 76.36 | 0.80 |
| Wed 27/May/2015 10:50:30 AM | 32822.4609 | -8.7 | 76.36 | 0.90 |
| Wed 27/May/2015 10:50:32 AM | 32822.4609 | -8.7 | 76.38 | 0.90 |
| Wed 27/May/2015 10:50:33 AM | 32822.4648 | -8.6 | 76.33 | 0.90 |
| Wed 27/May/2015 10:50:35 AM | 32822.4609 | -8.7 | 76.39 | 0.90 |
| Wed 27/May/2015 10:50:36 AM | 32822.4648 | -8.6 | 76.31 | 0.90 |
| Wed 27/May/2015 10:50:38 AM | 32822.4648 | -8.6 | 76.35 | 0.90 |
| Wed 27/May/2015 10:50:40 AM | 32822.4648 | -8.6 | 76.31 | 0.90 |
| Wed 27/May/2015 10:50:41 AM | 32822.4648 | -8.6 | 76.34 | 0.90 |
| Wed 27/May/2015 10:50:43 AM | 32822.4648 | -8.6 | 76.35 | 1.00 |
| Wed 27/May/2015 10:50:45 AM | 32822.4648 | -8.6 | 76.35 | 1.00 |
| Wed 27/May/2015 10:50:47 AM | 32822.4648 | -8.6 | 76.37 | 1.10 |
| Wed 27/May/2015 10:50:48 AM | 32822.4648 | -8.6 | 76.37 | 1.10 |
| Wed 27/May/2015 10:50:49 AM | 32822.4648 | -8.6 | 76.35 | 1.10 |
| Wed 27/May/2015 10:50:51 AM | 32822.4648 | -8.6 | 76.38 | 1.10 |
| Wed 27/May/2015 10:50:53 AM | 32822.4648 | -8.6 | 76.36 | 1.10 |
| Wed 27/May/2015 10:50:55 AM | 32822.4648 | -8.6 | 76.37 | 1.10 |
| Wed 27/May/2015 10:50:56 AM | 32822.4648 | -8.6 | 76.38 | 1.10 |
| Wed 27/May/2015 10:50:57 AM | 32822.4648 | -8.6 | 76.35 | 1.10 |
| Wed 27/May/2015 10:50:58 AM | 32822.4648 | -8.6 | 76.38 | 1.10 |
| Wed 27/May/2015 10:51:00 AM | 32822.4648 | -8.6 | 76.34 | 1.20 |
| Wed 27/May/2015 10:51:02 AM | 32822.4648 | -8.6 | 76.34 | 1.20 |
| Wed 27/May/2015 10:51:03 AM | 32822.4648 | -8.6 | 76.35 | 1.20 |
| Wed 27/May/2015 10:51:04 AM | 32822.4648 | -8.6 | 76.38 | 1.20 |
| Wed 27/May/2015 10:51:06 AM | 32822.4648 | -8.6 | 76.36 | 1.20 |
| Wed 27/May/2015 10:51:08 AM | 32822.4648 | -8.6 | 76.35 | 1.20 |
| Wed 27/May/2015 10:51:10 AM | 32822.4648 | -8.6 | 76.39 | 1.30 |
| Wed 27/May/2015 10:51:11 AM | 32822.4688 | -8.4 | 76.41 | 1.30 |
| Wed 27/May/2015 10:51:12 AM | 32822.4688 | -8.4 | 76.39 | 1.30 |
| Wed 27/May/2015 10:51:13 AM | 32822.4688 | -8.4 | 76.36 | 1.30 |
| Wed 27/May/2015 10:51:14 AM | 32822.4688 | -8.4 | 76.31 | 1.30 |
| Wed 27/May/2015 10:51:16 AM | 32822.4688 | -8.4 | 76.40 | 1.30 |
| Wed 27/May/2015 10:51:18 AM | 32822.4688 | -8.4 | 76.38 | 1.30 |
| Wed 27/May/2015 10:51:19 AM | 32822.4688 | -8.4 | 76.41 | 1.30 |
| Wed 27/May/2015 10:51:20 AM | 32822.4688 | -8.4 | 76.36 | 1.40 |
| Wed 27/May/2015 10:51:21 AM | 32822.4688 | -8.4 | 76.39 | 1.40 |
| Wed 27/May/2015 10:51:23 AM | 32822.4688 | -8.4 | 76.34 | 1.40 |
| Wed 27/May/2015 10:51:25 AM | 32822.4688 | -8.4 | 76.40 | 1.40 |
| Wed 27/May/2015 10:51:26 AM | 32822.4688 | -8.4 | 76.44 | 1.50 |
| Wed 27/May/2015 10:51:27 AM | 32822.4688 | -8.4 | 76.45 | 1.50 |
| Wed 27/May/2015 10:51:29 AM | 32822.4688 | -8.4 | 76.38 | 1.50 |
| Wed 27/May/2015 10:51:31 AM | 32822.4688 | -8.4 | 76.39 | 1.50 |


RTC Chip #1 Output Freq PPM vs. Temperature
RTC PPM
+40 PPM
-40 PPM
Current
RTC Output Frequency (PPM)
CURRENT (uA)
60
40
20
0
-20
-40
-60
180
160
140
120
100
80
60
40
20
0
0
20
40
60
80
100
120
140
160
180
200
Temperature °C (0C to 185C)


RTC Chip #1 Output Freq PPM vs. Temperature
RTC PPM
+40 PPM
-40 PPM
Current
RTC Output Frequency (PPM)
CURRENT (uA)
60
40
20
0
-20
-40
-60
180
160
140
120
100
80
60
40
20
0
120
125
130
135
140
145
150
155
160
165
170
175
Temperature °C (120C to 185C)

# Revision History

| ECO | REV | REVISION SUMMARY | PAGE | DATE |
|---|---|---|---|---|
| | - | Initial Release | | 05/02/2014 |
| 11539 | A | Update Frequency Stability Temperature Codes | | 06/08/15 |
| | | Rename P/N to QT1123L | | |