32.768kHz, 1MHz to 48MHz



18Vdc, 25Vdc, 33Vdc and 5.0Vdc

### **Description**

Q-Tech's Dual In-line (DIP) crystal oscillators are high-precision quartz crystal oscillators built in a metal through-hole package in a DIP-8 configuration.

### **Features**

- Made in the USA
- ECCN: EAR99
- DFARS 252-225-7014 Compliant: Electronic Component Exemption
- Wide frequency range from 1MHz to 48MHz
- · Wide operating temperature range
- CMOS Output Logic
- Supply voltages from 1.8Vdc to 5.0Vdc
- · All metal hermetically sealed package
- · Tight symmetry available
- · Fast rise and fall times
- · Fast start-up time
- High operating temperature up to +200°C
- Q-Tech does not use pure lead or pure tin in its products
- · RoHS compliant

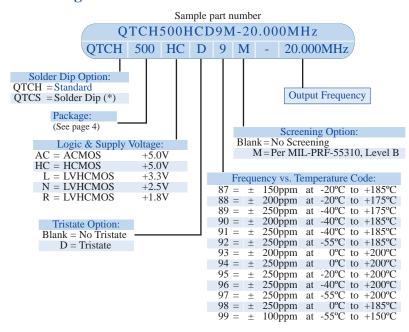


### **Applications**

- Wide military clock applications
- Smart munitions
- Navigation
- · Industrial controls
- · Microcontroller driver
- Down-hole applications up to +200°C



### **Ordering Information**



(\*) Hot Solder Dip Sn60/Pb40 per MIL-PRF 55310 is optional for an additional cost

For Non-Standard requirements, contact Q-Tech Corporation at Sales@Q-Tech.com

### **Packaging Options**

- Standard packaging in black foam
- Optional anti-static plastic tube

### Other Options Available For An Additional Charge

- Lead forming available on all packages. Please contact for details.
- P. I. N. D. test (MIL-STD 883, Method 2020)
- Lead trimming

All DIP packages are available in surface mount form. Specifications subject to change without prior notice.

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Q-TECH Corporation - 10150 W. Jefferson Boulevard, Culver City 90232 - Tel: 310-836-7900 - Fax: 310-836-2157 - www.q-tech.com



1.8Vdc, 2.5Vdc, 3.3Vdc and 5.0Vdc

### **Electrical Characteristics**

Parameters	R	N	L	AC/HC
Output frequency range (Fo) $\underline{1}$ /	1.000MHz - 48.000MHz			2.5MHz - 40.000MHz
Supply voltage (Vdd) <u>2</u> /	1.8Vdc ± 10%	2.5Vdc ± 10%	3.3Vdc ± 10%	5.0Vdc ± 10%
Maximum Applied Voltage (Vdd max.)	-0.3 to +4.0Vdc			-0.3 to +7.0Vdc
Frequency stability ( $\Delta F/\Delta T$ )	See Part Number on Page 1			
Operating temperature (Topr)	See Part Number on Page 1			
Storage temperature (Tsto)	-62°C to + 125°C			
Operating supply current (No Load)	1mA max.	1.5mA max.	2mA max.	7mA max.
Symmetry (50% of ouput waveform )	45/55%			
Rise and Fall times	бпѕ тах.			11ns max.
Output Load	15pF max.			
Start-up time (Tstup)	10ms max.			5ms max.
High Output Voltage (Voh)	0.9*Vdd min.			
Low Output Voltage (Vol)	0.1*Vdd max.			
Enable VIH Pin 1	VIH ≥ 0.7*Vdd (Active)			
Disable VIL Pin 1	VIL≤0.3*Vdd (High Impedance)			
Aging	±5ppm/first year			
Notes				

<sup>1/</sup>Full frequency range is not available in all packages. Consult factory for frequencies at 1MHz ~ 1.5MHz, and for frequencies greater than 48MHz.

<sup>2/</sup> For options R, D, and L, the part is designed to work from 1.8Vdc to 3.3Vdc. Supply voltage code is used to test the part to specific nominal voltage specified in a Purchase Order.



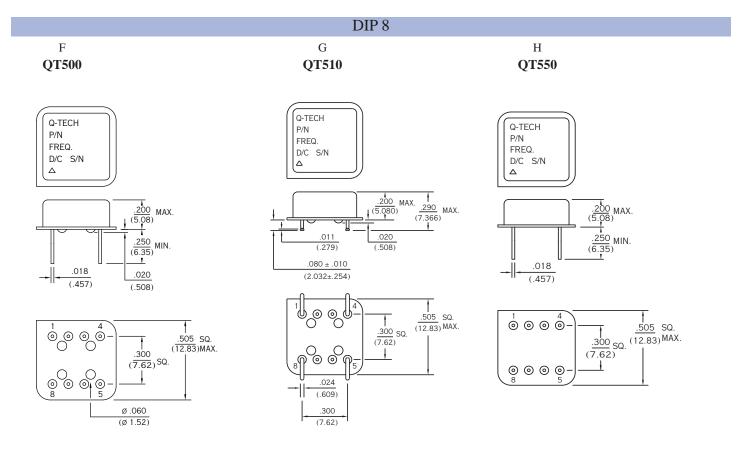
18Vdc, 25Vdc, 33Vdc and 5.0Vdc

## **Electrical Characteristics**

Parameters	N	L	
Output frequency range (Fo) 1/	32.768kHz		
Supply voltage (Vdd)	2.5Vdc ± 10%	$3.3$ Vdc $\pm 10\%$	
Maximum Applied Voltage (Vdd max.)	-0.3 to +'	7.0Vdc	
Frequency stability (ΔF/ΔT)	See Part Number on Page 1		
Operating temperature (Topr)	See Part Number on Page 1		
Storage temperature (Tsto)	-62°C to + 150°C		
Operating supply current (No Load)	70μA typ.   120μA max.		
Symmetry (50% of ouput waveform )	45% min   50% typ.   55% max.		
Rise and Fall times	50ns typ.   200ns max.		
Output Load	15pF max.		
Start-up time (Tstup)	10ms max.		
High Output Voltage (Voh)	0.9*Vdd min.		
Low Output Voltage (Vol)	0.1*Vdd max.		
Enable VIH Pin 1	VIH ≥ 0.7*Vdd Active		
Disable VIL Pin 1	VIL≤0.3*Vdd High Impedance		
Aging	±5ppm/first year		

# Package Outline and Pin Connections

**Dimensions are in inches (mm)** 



QT#	Vcc	GND	Case	Output	E/D or N/C
QT500	8	4	4	5	1
QT510	8	4	4	5	1
QT550	8	4	4	5	1

### **Package Information**

• Package material (header and leads): Kovar

• Lead finish: Gold Plated –  $50\mu \sim 80\mu$  inches Nickel Underplate –  $100\mu \sim 250\mu$  inches

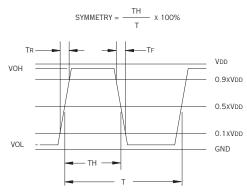
• Package to lid attachment: Resistance weld

• Cover: (DIP-8): Stainless Steel

• Weight: (DIP-8): 2.0g typ., 14.2g max.

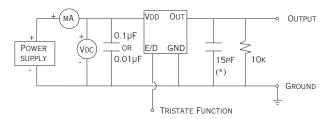


# **Output Waveform (Typical)**



### **Test Circuit**

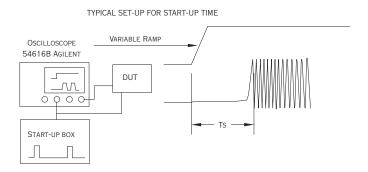
TYPICAL TEST CIRCUIT FOR CMOS LOGIC



(\*) CL INCLUDES PROBE AND JIG CAPACITANCE

The Tristate function on pin 1 has a built-in pull-up resistor typical  $10k\Omega$ , so it can be left floating or tied to Vdd without deteriorating the electrical performance.

# **Startup Time**





### **Thermal Characteristics**

The heat transfer model in a hybrid package is described in figure 1 (Based on single ASIC design).

Heat spreading occurs when heat flows into a material layer of increased cross-sectional area. It is adequate to assume that spreading occurs at a 45° angle.

The total thermal resistance is calculated by summing the thermal resistances of each material in the thermal path between the device and hybrid case.

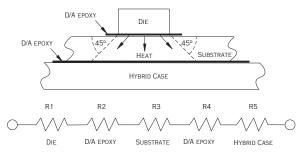
$$RT = R1 + R2 + R3 + R4 + R5$$

The total thermal resistance RT (see figure 2) between the heat source (die) to the hybrid case is the Theta Junction to Case (Theta JC) in °C/W.

- Theta junction to case (Theta JC) for this product is 24°C/W.
- Theta case to ambient (Theta CA) for this part is 105°C/W.
- Theta Junction to ambient (Theta JA) is 130°C/W.

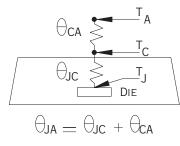
Maximum power dissipation PD for this package at 25°C is:

- PD(max) = (TJ (max) TA)/Theta JA
- With TJ = 175°C (Maximum junction temperature of die)
- PD(max) = (175 25)/130 = 1.15W



HIGH TEMPERATURE DUAL IN-LINE PACKAGE

(Figure 1)



(Figure 2)

### **Environmental Specifications**

Q-Tech Standard Screening/QCI (MIL-PRF55310) is available for all of our DIP packages. Q-Tech can also customize screening and test procedures to meet your specific requirements. The DIP packages are designed and processed to exceed the following test conditions:

Environmental Test	Test Conditions
Temperature cycling	MIL-STD-883, Method 1010, Cond. B
Constant acceleration	MIL-STD-883, Method 2001, Cond. A, Y1
Seal: Fine and Gross Leak	MIL-STD-883, Method 1014, Cond. A and C
Burn-in	160 hours, 125°C with load
Aging	30 days, 70°C, ± 0.7ppm max
Vibration sinusoidal	MIL-STD-202, Method 204, Cond. D
Shock, non operating	MIL-STD-202, Method 213, Cond. I
Thermal shock, non operating	MIL-STD-202, Method 107, Cond. B
Ambient pressure, non operating	MIL-STD-202, 105, Cond. C, 5 minutes dwell time minimum
Resistance to solder heat	MIL-STD-202, Method 210, Cond. C
Moisture resistance	MIL-STD-202, Method 106
Terminal strength	MIL-STD-202, Method 211, Cond. C
Resistance to solvents	MIL-STD-202, Method 215
Solderability	MIL-STD-202, Method 208
ESD Classification	MIL-STD-883, Method 3015, Class 1HBM 0 to 1,999V
Moisture Sensitivity Level	J-STD-020, MSL=1

Please contact Q-Tech for higher shock requirements



# HIGH TEMPERATURE DUAL IN-LINE PACKAGE

CRYSTAL CLOCK OSCILLATORS

32.768kHz, 1MHz to 48MHz

18Vdc, 25Vdc, 33Vdc and 5.0Vdc

DCO	REV	REVISION SUMMARY	PAGE	DATE
13279	-	Initial Release	All	03/25/2021

QPDS-0153 (Revision -, March 2021)

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