

Description

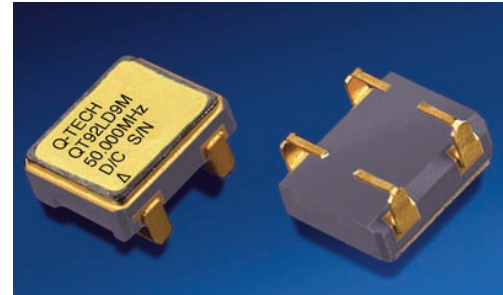
Q-Tech's surface-mount QT92 Series oscillators consist of an IC 5Vdc, 3.3Vdc, 2.5Vdc, 1.8Vdc clock square wave generator and a round AT high-precision quartz crystal built in a rugged surface-mount ceramic miniature package. It was designed to be replaceable and retrofitable into the footprint of a 7 x 5mm COTS oscillator.

Features

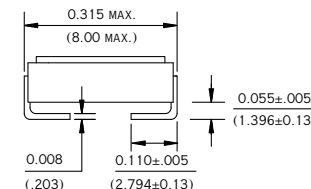
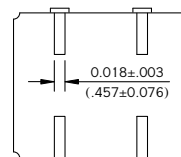
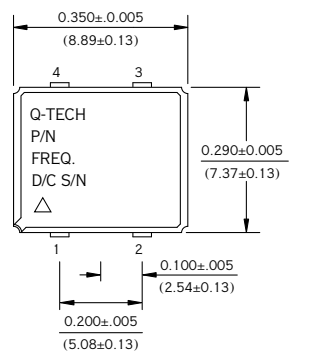
- Made in the USA
- ECCN: EAR99
- DFARS 252-225-7014 Compliant:
Electronic Component Exemption
- **Drop in replacement for 7 x 5mm COTS oscillator with built-in by-pass capacitor**
- **Smallest AT round crystal package ever designed**
- Available as QPL MIL-PRF-55310/37 and /38
- Able to meet 36000G shock per ITOP 1-2-601
- Radiation tolerant to 10K RAD
- Broad frequency range from 15kHz to 160MHz
- Rugged 4 point mount design for high shock and vibration
- ACMOS, HCMOS, TTL or LVHCMOS logic
- Tri-State Output Option (D)
- Hermetically sealed ceramic SMD package
- Fundamental and 3rd Overtone designs
- Low phase noise
- Custom designs available
- Q-Tech does not use pure lead or pure tin in its products

Applications

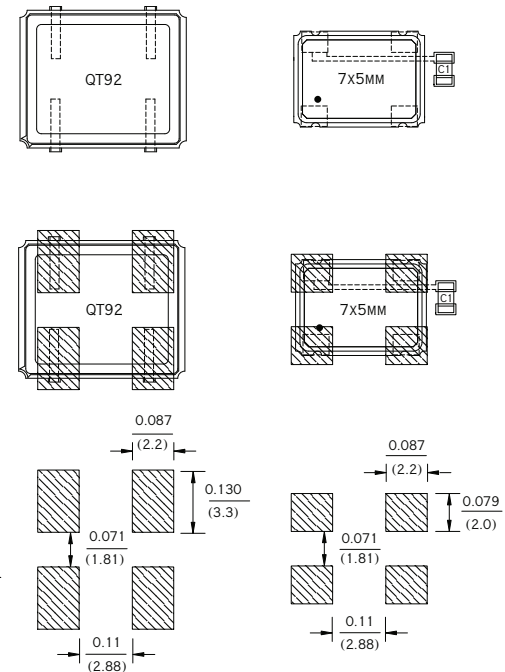
- Designed to meet today's requirements for low voltage applications
- Wide military clock applications
- Gun launched munitions and systems
- Benign space environments
- Smart munitions
- Navigation
- Industrial controls
- Microcontroller driver
- Down-hole applications up to +200°C



Package Specifications and Outline



Layout comparison of QT92 vs. 7x5mm



Pin No.	Function
1	TRISTATE or NC
2	GND/CASE
3	OUTPUT
4	VDD

Dimensions are in inches (mm)

Package Information

- Package material: 90% AL₂O₃
- Lead material: Kovar
- Lead finish: Gold Plated: 50μ ~ 80μ inches
Nickel Underplate: 100μ ~ 250μ inches
- Weight: 0.6g typ., 3.0g max.



Electrical Characteristics

Parameters	QT92AC	QT92HC	QT92T	QT92L	QT92N	QT92R	
Output frequency range (Fo)	500kHz — 85.000MHz	15kHz — 85.000MHz(*)	500kHz — 85.000MHz	125kHz — 160.000MHz (*)	125.000kHz — 133.000MHz	125.000kHz — 100.000MHz	
Supply voltage (Vdd)	5.0Vdc ± 10%			3.3Vdc ± 10%		1.8Vdc ± 10%	
Maximum Applied Voltage (Vdd max.)	-0.5 to +7.0Vdc			-0.5 to +5.0Vdc			
Frequency stability (ΔF/ΔT)	See Option codes						
Operating temperature (Topr)	See Option codes						
Storage temperature (Tsto)	-62°C to +125°C						
Operating supply current (Idd) (No Load)	20 mA max. - 15kHz ~ < 16MHz 25 mA max. - 16MHz ~ < 32MHz 35 mA max. - 32MHz ~ < 60MHz 45 mA max. - 60MHz ~ < 85MHz			3 mA max. - 125kHz ~ < 500kHz 6 mA max. - 500kHz ~ < 16MHz 10 mA max. - 16MHz ~ < 32MHz 20 mA max. - 32MHz ~ < 60MHz 30 mA max. - 60MHz ~ < 100MHz 40 mA max. - 100MHz ~ < 130MHz 50 mA max. - 130MHz ~ ≤ 160MHz		3 mA max. - 125kHz ~ < 500kHz 6 mA max. - 500kHz ~ < 40MHz 15 mA max. - 40MHz ~ < 60MHz 25 mA max. - 60MHz ~ < 85MHz 35 mA max. - 85MHz ~ ≤ 133MHz	4 mA max. - 125kHz ~ < 40MHz 10 mA max. - 40MHz ~ < 50MHz 20 mA max. - 50MHz ~ < 85MHz 25 mA max. - 85MHz ~ ≤ 100MHz
Symmetry (50% of output waveform or 1.4Vdc for TTL)	45/55% max. - 15kHz ~ < 16MHz 40/60% max. - 16 ~ ≤ 85MHz (Tighter symmetry available)			45/55% max. - 125kHz ~ < 16MHz 40/60% max. - 16 ~ ≤ 160MHz (Tighter symmetry available)		45/55% max. - 125kHz ~ < 16MHz 40/60% max. - 16 ~ ≤ 133MHz (Tighter symmetry available)	45/55% max. - 125kHz ~ < 16MHz 40/60% max. - 16 ~ ≤ 100MHz (Tighter symmetry available)
Rise and Fall times (with typical load)	6ns max. - Fo < 30MHz 3ns max. - Fo ≥ 30 - 85MHz (between 10% to 90%)	6ns max. - Fo < 30MHz 3ns max. - Fo ≥ 30 - 85MHz (between 10% to 90%)	5ns max. - Fo < 30MHz 3ns max. - Fo ≥ 30 - 85MHz (between 0.8V to 2.0V)	6ns max. - 125kHz ~ < 40MHz 3ns max. - 40 ~ ≤ 160MHz (between 10% to 90%)	5ns max. - 125kHz ~ < 40MHz 3ns max. - 40 ~ ≤ 133MHz (between 10% to 90%)	5ns max. - 125kHz ~ < 40MHz 3ns max. - 40 ~ ≤ 100MHz (between 10% to 90%)	
Output Load	15pF // 10kohms 50pF max. or 10TTL for (Fo < 60MHz) 30pF max. or 6TTL for (Fo ≥ 60MHz)	15pF // 10kohms (2LSTTL)	10TTL (Fo < 60MHz) 6TTL (Fo ≥ 60MHz)	15pF // 10kohms (30pF max. for F ≤ 50MHz)	15pF // 10kohms		
Start-up time (Tstup)	5ms max.						
Output voltage (Voh/Vol)	0.9 x Vdd min.; 0.1 x Vdd max.			2.4V min.; 0.4V max.		0.9 x Vdd min.; 0.1 x Vdd max.	
Output Current (Ioh/Iol)	± 24mA max.	± 8mA max.	-1.6 mA/TTL +40 μA/TTL	± 4mA max.			
Enable/Disable Tristate function Pin 1	VIH ≥ 2.2V Oscillation; VIL ≤ 0.8V High Impedance				VIH ≥ 0.7 x Vdd Oscillation; VIL ≤ 0.3 x Vdd High Impedance		
Jitter RMS 1σ (at 25°C)	8ps typ. - < 40MHz 5ps typ. - ≥ 40MHz			15ps typ. - < 40MHz 8ps typ. - ≥ 40MHz			
Aging (at 70°C)	± 5ppm max. first year / ± 2ppm max. per year thereafter						

(*) Some frequencies lower than 500kHz may not be available with tristate function

Ordering Information

5.0Vdc

Sample part number

QT92HCD9M-85.000MHz

Q T 92 H C D 9 M - 85.000MHz

T = Standard
S = Solder Dip (*)

Logic:
AC = AC MOS
HC = HCMOS
T = TTL

Tristate Option
Blank = No Tristate
D = Tristate

Output frequency

Screening Options:
Blank = No Screening
M = Per MIL-PRF-55310, Level B

1	= ±	100ppm	at	0°C	to	+70°C
4	= ±	50ppm	at	0°C	to	+70°C
5	= ±	25ppm	at	-20°C	to	+70°C
6	= ±	50ppm	at	-55°C	to	+105°C
9	= ±	50ppm	at	-55°C	to	+125°C
10	= ±	100ppm	at	-55°C	to	+125°C
11	= ±	50ppm	at	-40°C	to	+85°C
12	= ±	100ppm	at	-40°C	to	+85°C
14	= ±	20ppm	at	-20°C	to	+70°C
15	= ±	25ppm	at	-40°C	to	+85°C

3.3Vdc

Sample part number

QT92LD6M-150.000MHz

Q T 92 L D 6 M - 150.000MHz

T = Standard
S = Solder Dip (*)

Tristate Option
Blank = No Tristate
D = Tristate

Output frequency

Screening Options:
Blank = No Screening
M = Per MIL-PRF-55310, Level B

1	= ±	100ppm	at	0°C	to	+70°C
4	= ±	50ppm	at	0°C	to	+70°C
5	= ±	25ppm	at	-20°C	to	+70°C
6	= ±	50ppm	at	-55°C	to	+105°C
9	= ±	50ppm	at	-55°C	to	+125°C
10	= ±	100ppm	at	-55°C	to	+125°C
11	= ±	50ppm	at	-40°C	to	+85°C
12	= ±	100ppm	at	-40°C	to	+85°C
14	= ±	20ppm	at	-20°C	to	+70°C
15	= ±	25ppm	at	-40°C	to	+85°C

2.5Vdc

Sample part number

QT92ND12M-133.000MHz

Q T 92 N D 12 M - 133.000MHz

T = Standard
S = Solder Dip (*)

Tristate Option
Blank = No Tristate
D = Tristate

Output frequency

Screening Options:
Blank = No Screening
M = Per MIL-PRF-55310, Level B

1	= ±	100ppm	at	0°C	to	+70°C
4	= ±	50ppm	at	0°C	to	+70°C
5	= ±	25ppm	at	-20°C	to	+70°C
6	= ±	50ppm	at	-55°C	to	+105°C
9	= ±	50ppm	at	-55°C	to	+125°C
10	= ±	100ppm	at	-55°C	to	+125°C
11	= ±	50ppm	at	-40°C	to	+85°C
12	= ±	100ppm	at	-40°C	to	+85°C
14	= ±	20ppm	at	-20°C	to	+70°C
15	= ±	25ppm	at	-40°C	to	+85°C

1.8Vdc

Sample part number

QT92RD1M-100.000MHz

Q T 92 R D 1 M - 100.000MHz

T = Standard
S = Solder Dip (*)

Tristate Option
Blank = No Tristate
D = Tristate

Output frequency

Screening Options:
Blank = No Screening
M = Per MIL-PRF-55310, Level B

1	= ±	100ppm	at	0°C	to	+70°C
4	= ±	50ppm	at	0°C	to	+70°C
5	= ±	25ppm	at	-20°C	to	+70°C
6	= ±	50ppm	at	-55°C	to	+105°C
9	= ±	50ppm	at	-55°C	to	+125°C
10	= ±	100ppm	at	-55°C	to	+125°C
11	= ±	50ppm	at	-40°C	to	+85°C
12	= ±	100ppm	at	-40°C	to	+85°C
14	= ±	20ppm	at	-20°C	to	+70°C
15	= ±	25ppm	at	-40°C	to	+85°C

Frequency stability vs. temperature codes may not be available in all frequencies.

For Non-Standard requirements, contact Q-Tech Corporation at Sales@Q-Tech.com

Packaging Options

- Standard packaging in anti-static plastic tube (60pcs/tube)
- Tape and Reel (800pcs/reel) is available for an additional charge.

Other Options Available For An Additional Charge

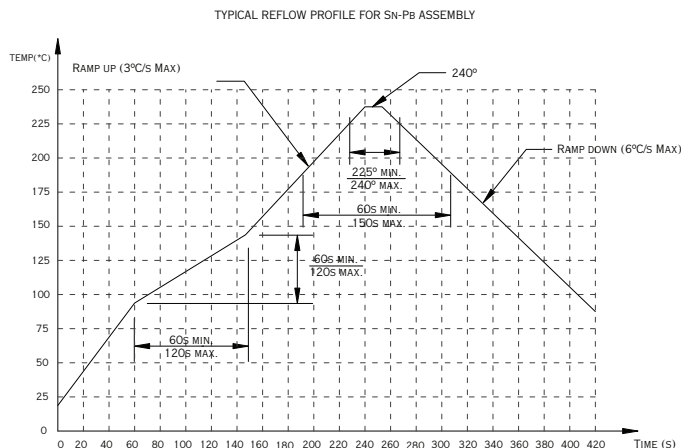
- (*) Hot Solder Dip Sn60 per MIL-PRF 55310
- P. I. N. D. test (MIL-STD 883, Method 2020)

Specifications subject to change without prior notice.

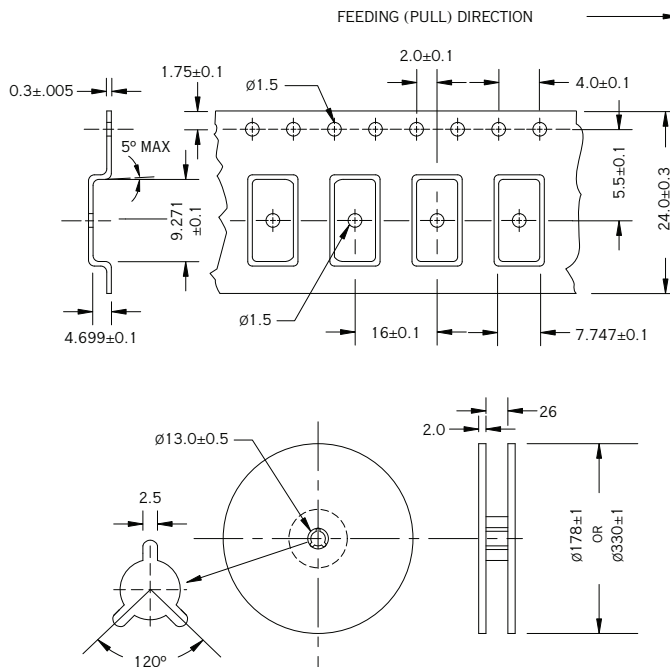
Reflow Profile

The five transition periods for the typical reflow process are:

- Preheat
- Flux activation
- Thermal equalization
- Reflow
- Cool down



Embossed Tape and Reel Information For QT92



Dimensions are in mm. Tape is compliant to EIA-481-A.

Reel size vs. quantity:

Reel size (Diameter in mm)	Qty per reel (pcs)
178	150
330	800

Environmental Specifications

Q-Tech Standard Screening/QCI (MIL-PRF55310) is available for all of our QT92 Products. Q-Tech can also customize screening and test procedures to meet your specific requirements. The QT92 product is designed and processed to exceed the following test conditions:

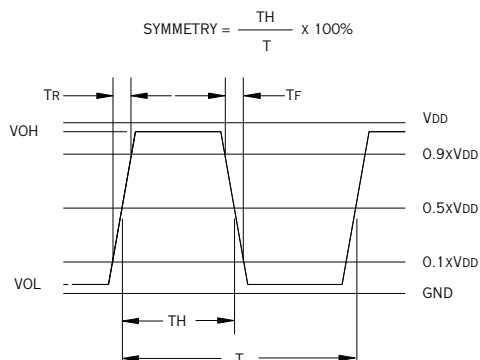
Environmental Test	Test Conditions
Temperature cycling	MIL-STD-883, Method 1010, Cond. B
Constant acceleration	MIL-STD-883, Method 2001, Cond. A, Y1
Seal: Fine and Gross Leak	MIL-STD-883, Method 1014, Cond. A and C
Burn-in	160 hours, 125°C with load
Aging	30 days, 70°C, ±1.5ppm max
Vibration sinusoidal	MIL-STD-202, Method 204, Cond. D
Shock, non operating	MIL-STD-202, Method 213, Cond. I (See Note 1)
Thermal shock, non operating	MIL-STD-202, Method 107, Cond. B
Ambient pressure, non operating	MIL-STD-202, 105, Cond. C, 5 minutes dwell time minimum
Resistance to solder heat	MIL-STD-202, Method 210, Cond. C
Moisture resistance	MIL-STD-202, Method 106
Terminal strength	MIL-STD-202, Method 211, Cond. C
Resistance to solvents	MIL-STD-202, Method 215
Solderability	MIL-STD-202, Method 208
ESD Classification	MIL-STD-883, Method 3015, Class 1 HBM 0 to 1,999V
Moisture Sensitivity Level	J-STD-020, MSL=1

Note 1: Additional shock results successfully passed on standard QT88 family 16MHz, 20MHz, 24MHz, 40MHz, and 80MHz

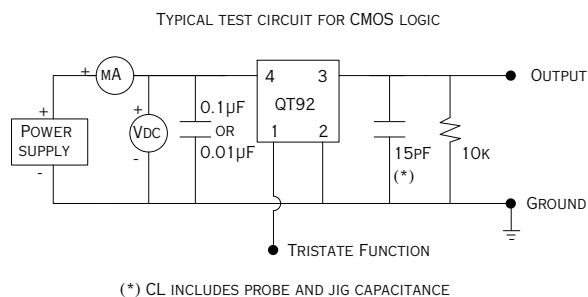
- Shock 850g peak, half-sine, 1 ms duration (MIL-STD-202, Method 213, Cond. D modified)
- Shock 1,500g peak, half-sine, 0.5ms duration (MIL-STD-883, Method 2002, Cond. B)
- Shock 36,000g peak, half-sine, 0.12 ms duration

Please contact Q-Tech for higher shock requirements

Output Waveform (Typical)

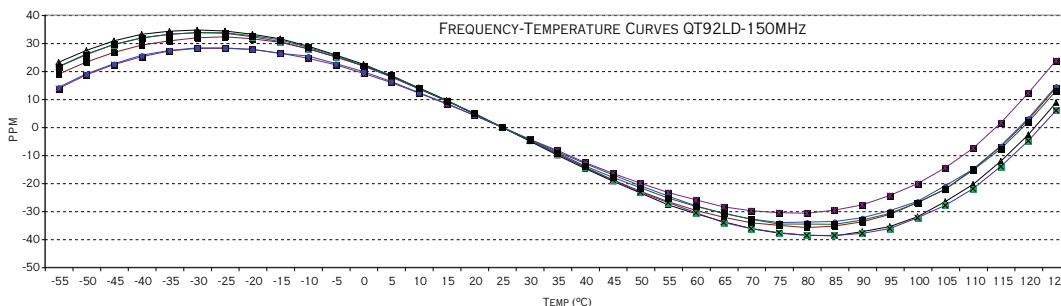


Test Circuit



The Tristate function on pin 1 has a built-in pull-up resistor typical 50kΩ, so it can be left floating or tied to Vdd without deteriorating the electrical performance.

Frequency vs. Temperature Curve



Thermal Characteristics

The heat transfer model in a hybrid package is described in figure 1.

Heat spreading occurs when heat flows into a material layer of increased cross-sectional area. It is adequate to assume that spreading occurs at a 45° angle.

The total thermal resistance is calculated by summing the thermal resistances of each material in the thermal path between the device and hybrid case.

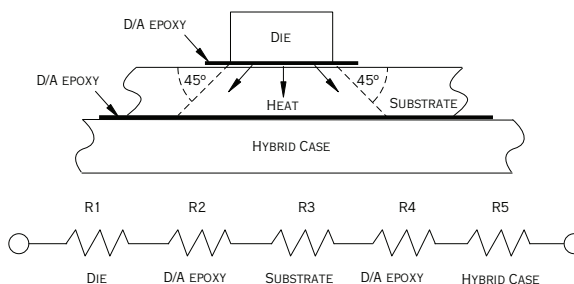
$$RT = R1 + R2 + R3 + R4 + R5$$

The total thermal resistance RT (see figure 2) between the heat source (die) to the hybrid case is the Theta Junction to Case (Theta JC) in °C/W.

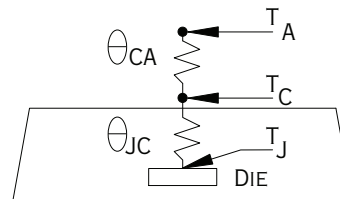
- Theta junction to case (Theta JC) for this product is 30°C/W.
- Theta case to ambient (Theta CA) for this part is 100°C/W.
- Theta Junction to ambient (Theta JA) is 130°C/W.

Maximum power dissipation PD for this package at 25°C is:

- $PD(max) = (T_J(max) - T_A) / \theta_{JA}$
- With $T_J = 175^\circ C$ (Maximum junction temperature of die)
- $PD(max) = (175 - 25) / 130 = 1.15W$



(Figure 1)

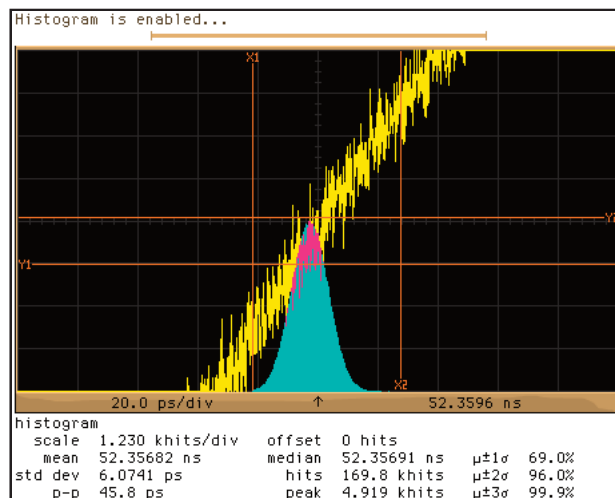


$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$

(Figure 2)

Period Jitter

As data rates increase, effects of jitter become critical with its budgets tighter. Jitter is the deviation of a timing event of a signal from its ideal position. Jitter is complex and is composed of both random and deterministic jitter components. Random jitter (RJ) is theoretically unbounded and Gaussian in distribution. Deterministic jitter (DJ) is bounded and does not follow any predictable distribution. DJ is also referred to as systematic jitter. A technique to measure period jitter (RMS) one standard deviation (1σ) and peak-to-peak jitter in time domain is to use a high sampling rate (>8G samples/s) digitizing oscilloscope. Figure shows an example of peak-to-peak jitter and RMS jitter (1σ) of a QT92ND-100MHz, at 2.5Vdc.



Phase Noise and Phase Jitter Integration

RMS jitter (1σ): 6.07ps Peak-to-peak jitter: 45.8ps

Phase noise is measured in the frequency domain, and is expressed as a ratio of signal power to noise power measured in a 1Hz bandwidth at an offset frequency from the carrier, e.g. 10Hz, 100Hz, 1kHz, 10kHz, 100kHz, etc. Phase noise measurement is made with an Agilent E5052A Signal Source Analyzer (SSA) with built-in outstanding low-noise DC power supply source. The DC source is floated from the ground and isolated from external noise to ensure accuracy and repeatability.

In order to determine the total noise power over a certain frequency range (bandwidth), the time domain must be analyzed in the frequency domain, and then reconstructed in the time domain into an rms value with the unwanted frequencies excluded. This may be done by converting $L(f)$ back to $S\phi(f)$ over the bandwidth of interest, integrating and performing some calculations.

Symbol	Definition
$\int L(f)$	Integrated single side band phase noise (dBc)
$S\phi(f) = (180/\pi) \times \sqrt{2} \int L(f) df$	Spectral density of phase modulation, also known as RMS phase error (in degrees)
RMS jitter = $S\phi(f) / (f_{osc} \cdot 360^\circ)$	Jitter (in seconds) due to phase noise. Note $S\phi(f)$ in degrees.

The value of RMS jitter over the bandwidth of interest, e.g. 10kHz to 20MHz, 10Hz to 20MHz, represents 1 standard deviation of phase jitter contributed by the noise in that defined bandwidth.

Figure below shows a typical Phase Noise/Phase jitter of a QT92HCD, 5.0Vdc, 40MHz clock at offset frequencies 10Hz to 5MHz, and phase jitter integrated over the bandwidth of 12kHz to 1MHz.

