Clock Termination Techniques and Load sensitivities in Crystal Oscillators

APPLICATION NOTES QTAN-105

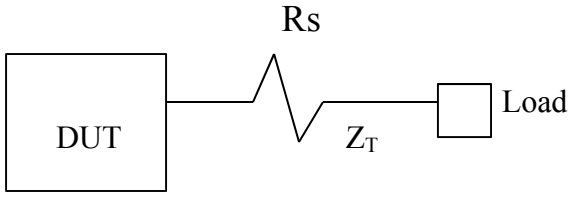
Due to the fast transition of the ACMOS and low impedance outputs, proper termination techniques must be used when the devices are used to drive loads with large impedances causing a mismatch in impedance.
Termination is usually used to solve the problem of voltage reflections, which essentially cause steps in clock waveforms as well as overshoot and undershoot. Such effect could result in false clocking of data, as well as higher EMI and system noise.
Termination is required also due to the length of the PCB trace and the load configuration.
There are three general methods of terminating a clock trace, which is a process of matching the output impedance of the device with the line impedance:

- Series termination
- Pull-up/Pull-down termination
- Parallel AC termination

METHOD 1: SERIES TERMINATION

In series termination, a damping resistor is placed close to the source of the clock signal. Value of Rs must satisfy the following requirement:

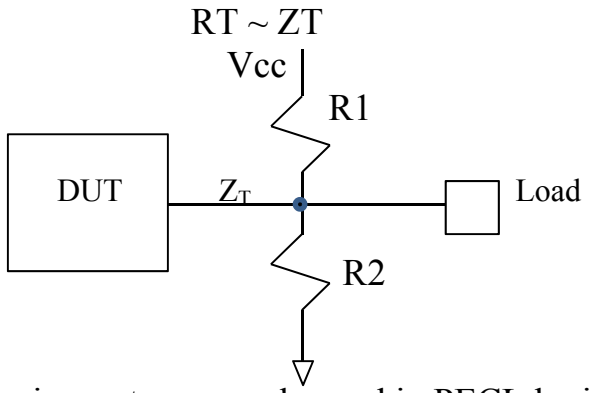
$$Rs \geq ZT - Ro$$



Most Q-Tech oscillators have a built-in series resistor with typical value between 10Ω and 50Ω. If additional resistor is needed, the resistor should be placed as close to the clock source as possible. A large value resistor may increase rise and fall time and is load and frequency dependent.

METHOD 2: PULL-UP/PULL-DOWN TERMINATION

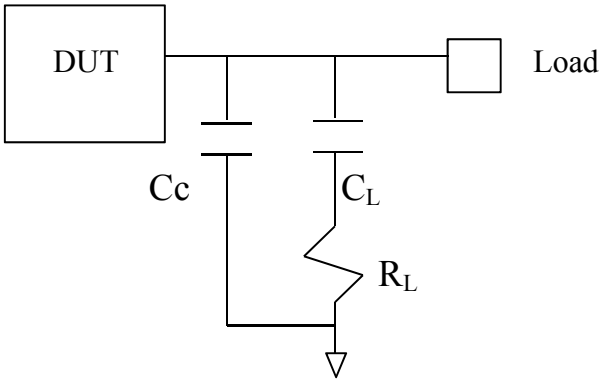
In pull-up/pull-down termination, the Thevenin's equivalent of the combination is equal to the characteristics impedance of the trace. This is probably the cleanest resulting in no reflection and EMI.

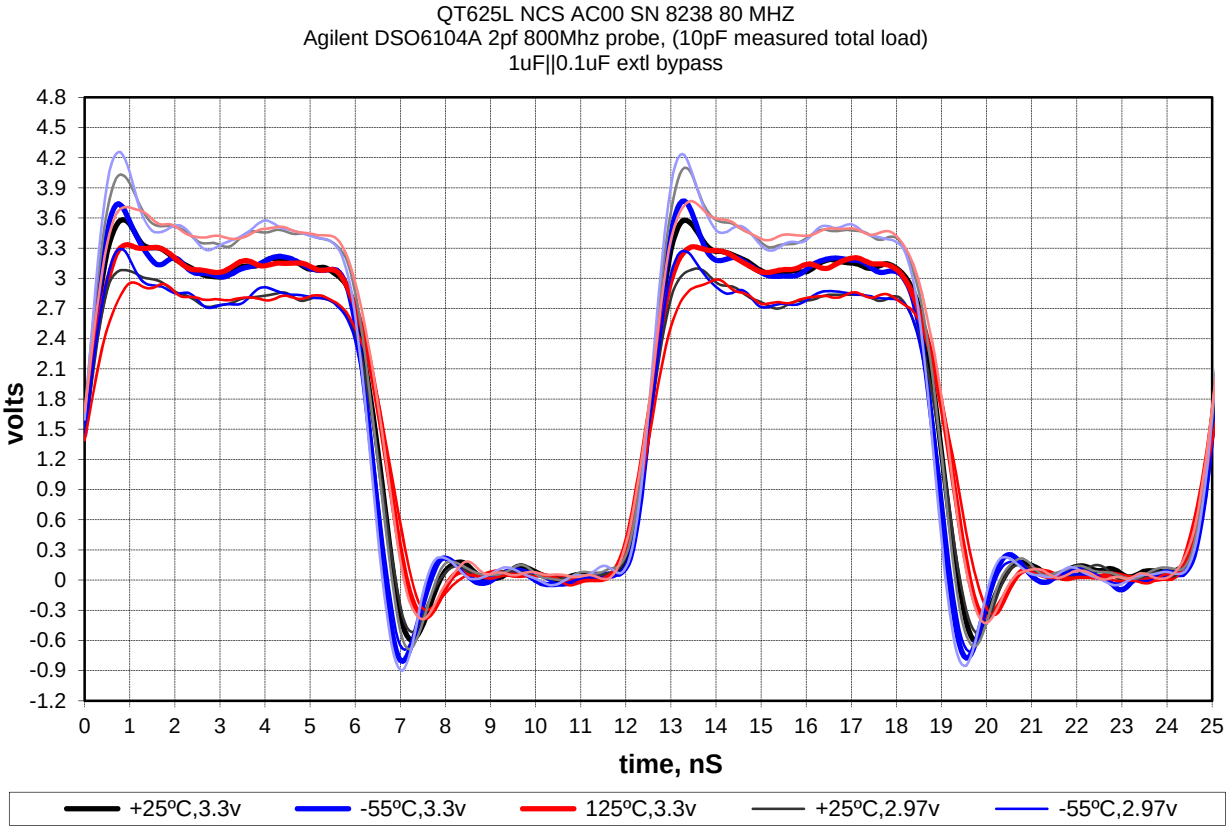


The Thevenin termination is most commonly used in PECL logic where the load impedance is 50Ω.

METHOD 3: PARALLEL TERMINATION

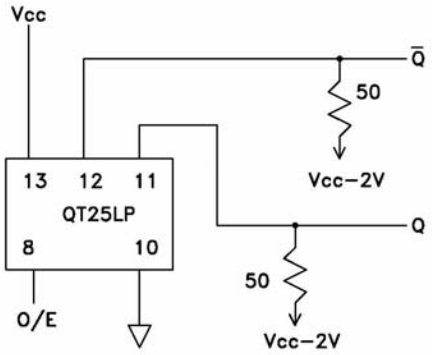
In parallel termination, a R-C combination is placed at the load. The value of the capacitor must be chosen carefully, usually smaller than 50pF. This termination is not recommended because it will degrade the rise and fall time of the clock, although it draws no DC current.



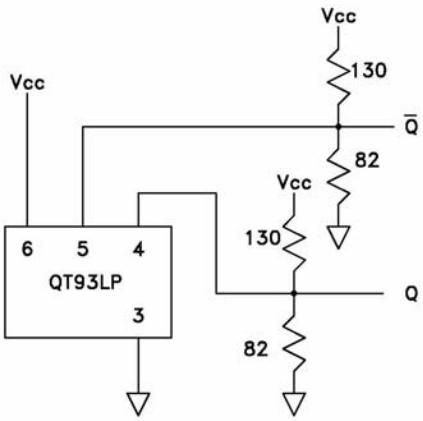


LVPECL and LVDS

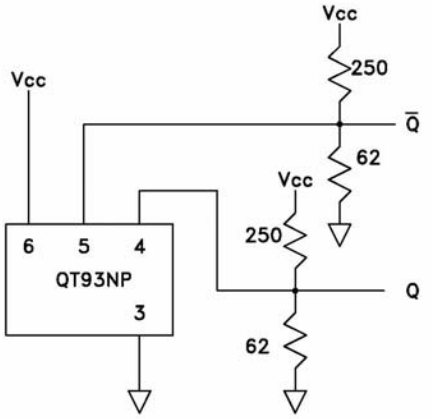
LVPECL and LVDS logic outputs provided superior advantages over HCMOS and TTL technology with low cost, high speed fast rise and fall times, low power and low jitter. The LVDS has the lowest differential swing with a typical voltage swing of 350mV with a typical offset voltage of 1.25V above ground.



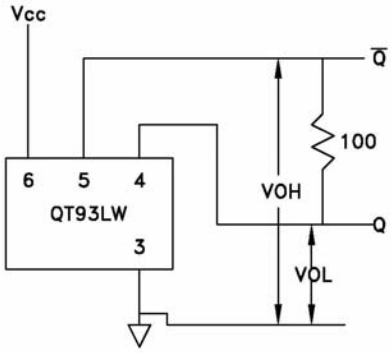
STANDARD TERMINATION LVPECL



THEVENIN EQUIVALENT 3.3V LVPECL



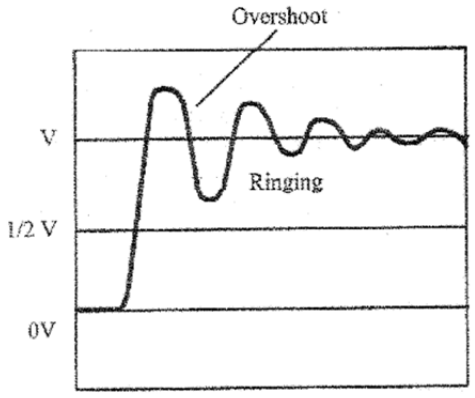
THEVENIN EQUIVALENT 2.5V LVPECL



LVDS TERMINATION

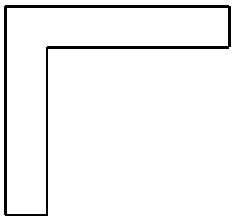
CRITICAL GUIDELINES FOR PCB

- The RF signals are highly sensitive to noise. The possibility of incurring ringing and reflections must be treated with care.
- Impedance matching is extremely critical for RF. The PCB designer must consider keeping the line impedance ay 50Ω; 50Ω out from the driver, 50Ω during transmission, and 50Ω into the receiver.
- The return loss must be minimized. This loss is caused by signal reflection, or ringing. The return is the path taken by the return current.

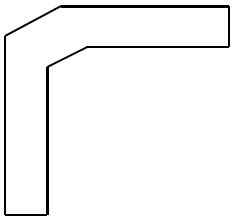


Ringing created by impedance mismatch on a transmission line

- Add decoupling capacitors between Vcc and ground and place them near the Vcc power of the clock oscillator. The decoupling capacitors are required to reduce noise that may be transmitted to the clock signal.
- Keep the crosstalk factor in mind. As the system performance and board densities increase, the problem of cross talk and how to deal with it becomes more important. Cross talk is the transfer of energy between adjacent conductors due to mutual inductance and shunt capacitance.
- Also keep the signal traces as far apart as possible.
- The distance that the lines run parallel to eah other should be kept to a minimum.
- Avoid 90° right angle bends in a trace. Try to keep traces straight unless necessary or keep at 45° cut traces.



Avoid 90° right angle bends



Use 45° angle bends

- Differential traces between Q and QNOT of LVDS or LVPECL should be equal in length to avoid impedance mismatch and different propagation delay times.