

### Description

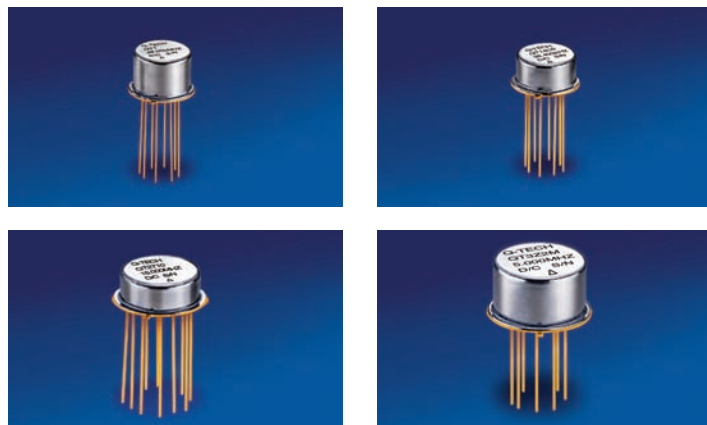
Q-Tech's Transistor Outline package crystal oscillators consist of a source clock square wave generator, logic output buffers and/or logic divider stages, and a round AT high-precision quartz crystal built in an all metal TO package.

### Features

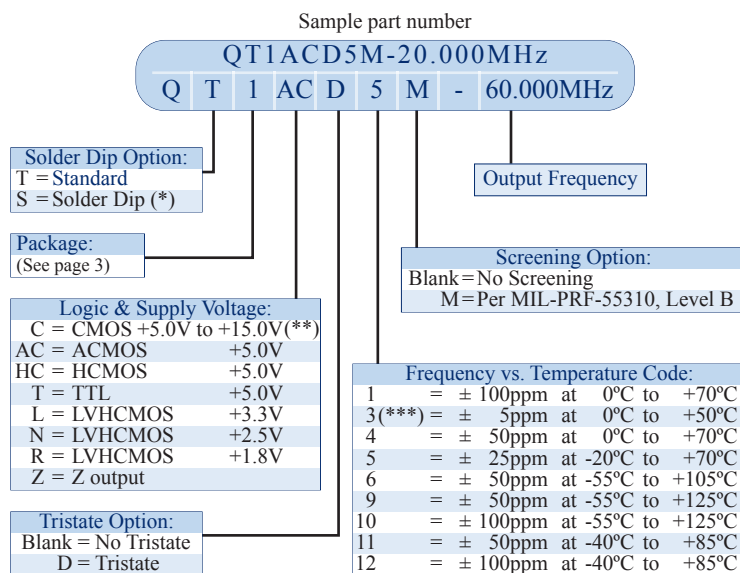
- Made in the USA
- ECCN: EAR99
- DFARS 252-225-7014 Compliant: Electronic Component Exemption
- Wide frequency range from 0.045Hz to 125MHz
- Available as QPL MIL-PRF-55310/09 and/10 (TTL) and /12 (CMOS)
- Choice of TO packages and pin outs
- Choice of supply voltages
- Choice of output logic options ( CMOS, ACMOS, HCMOS, LVHCMOS, and TTL)
- AT-Cut crystal
- All metal hermetically sealed package
- Tight or custom symmetry available
- Low height available
- External tuning capacitor option
- Fundamental and third overtone designs
- Tristate function option D
- Three-point crystal mounts
- Custom design available tailors to meet customer's needs
- Q-Tech does not use pure lead or pure tin in its products

### Applications

- Designed to meet today's requirements for all voltage applications
- Wide military clock applications
- Industrial controls
- Microcontroller driver



### Ordering Information



(\*) Hot Solder Dip Sn60/Pb40 per MIL-PRF 55310 is optional for an additional cost

(\*\*) Please specify supply voltage when ordering CMOS

(\*\*\*) Requires an external capacitor

For frequency stability vs. temperature options not listed herein, please request a custom part number.

For Non-Standard requirements, contact Q-Tech Corporation at  
Sales@Q-Tech.com

### Packaging Options

- Standard packaging in black foam

### Other Options Available For An Additional Charge

- P. I. N. D. test (MIL-STD 883, Method 2020)
- Lead trimming

All Transistor Outline packages are available in surface mount form.

Specifications subject to change without prior notice.



**TRANSISTOR OUTLINE PACKAGES**  
**TO-5 and TO-8 CRYSTAL CLOCK OSCILLATORS**  
**1.8 to 15Vdc - 0.045Hz to 125MHz**

**Electrical Characteristics**

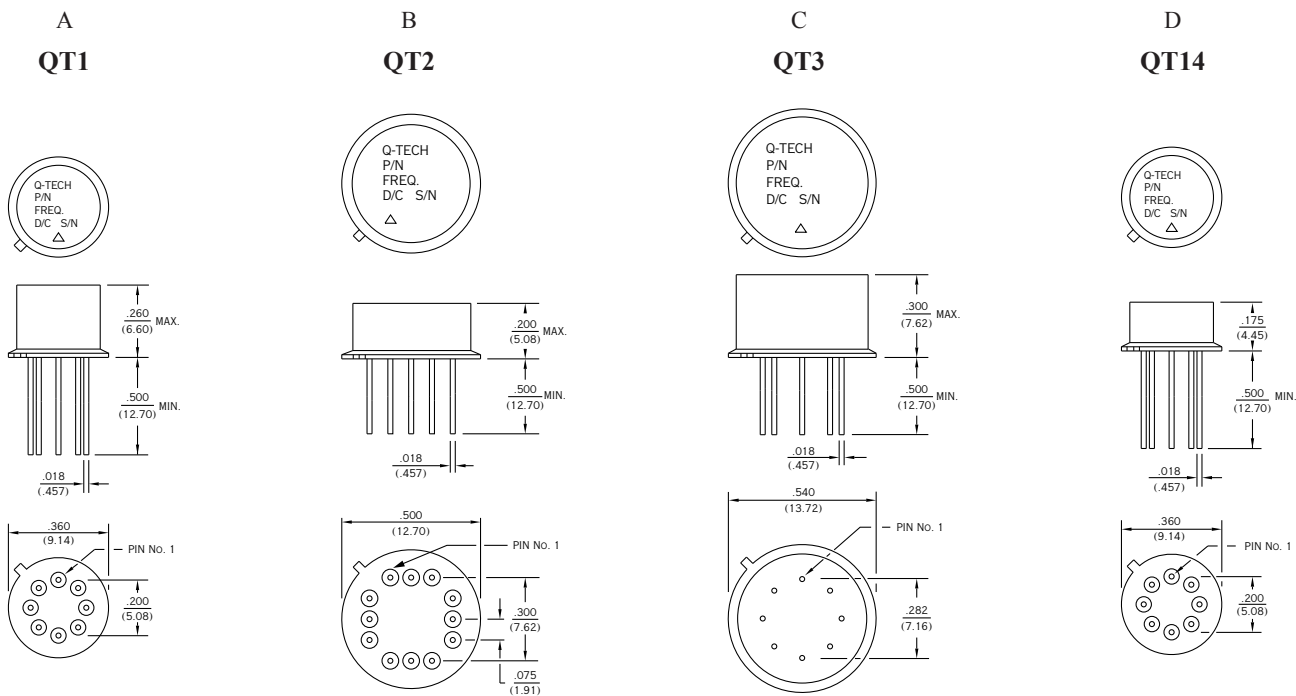
Parameters		C	AC	HC	T	L (*)
Output freq. range (Fo)	QT1, 14	244Hz — 15MHz	732.4Hz — 85MHz		732.4Hz — 125MHz	
	QT2		0.045Hz — 85MHz		0.045Hz — 85MHz	
	QT3		732.4Hz — 85MHz		732.4Hz — 85MHz	
Supply voltage (Vdd)	5V ~ 15Vdc ± 10%		5.0Vdc ± 10%		3.3Vdc ± 10%	
Maximum Applied Voltage (Vdd max.)	-0.5 to +18Vdc		-0.5 to +7.0Vdc		-0.5 to +5.0Vdc	
Freq. stability (ΔF/ΔT)			See Option codes			
Operating temp. (Topr)			See Option codes			
Storage temp. (Tsto)			-62°C to + 125°C			
Operating supply current (Idd) (No Load)	F and Vdd dependent 3 mA max. at 5V up to 5MHz 25 mA max. at 15V up to 15MHz		20 mA max. - 0.045Hz ~ < 16MHz 25 mA max. - 16MHz ~ < 40MHz 35 mA max. - 40MHz ~ < 60MHz 45 mA max. - 60MHz ~ 85MHz		3 mA max. - 0.045Hz ~ < 500kHz 6 mA max. - 500kHz ~ < 16MHz 10 mA max. - 16MHz ~ < 32MHz 20 mA max. - 32MHz ~ < 60MHz 30 mA max. - 60MHz ~ < 100MHz 40 mA max. - 100MHz ~ 125MHz	
Symmetry (50% of output waveform or 1.4Vdc for TTL)	45/55% max. Fo < 4MHz 40/60% max. Fo ≥ 4MHz		45/55% max. Fo < 12MHz 40/60% max. Fo ≥ 12MHz			
Rise and Fall times (with typical load)	30ns max.  (Measured from 10% to 90%)		15ns max. Fo < 15kHz 6ns max. Fo 15kHz ~ 39.999MHz 3ns max. Fo 40MHz ~ 125 MHz (Measured from 10% to 90% CMOS or from 0.8V to 2.0V TTL)			
Output Load	15pF // 10kΩ			10TTL Fo < 20MHz 6TTL Fo ≥ 20MHz	15pF // 10kΩ	
Start-up time (Tstup)	10ms max.					
Output voltage (Voh/Vol)	0.9 x Vdd min.; 0.1 x Vdd max.			2.4V min.; 0.4V max.	0.9 x Vdd min.; 0.1 x Vdd max.	
Output Current (Ioh/Iol)	± 1mA typ. at 5V ± 6.8mA typ. at 15V		± 24mA	± 8 mA	-1.6mA / TTL +40μA / TTL	± 4mA .
Enable/Disable Tristate function Pin 1	Call for details		VIH ≥ 2.2V Oscillation; VIL ≤ 0.8V High Impedance		VIH ≥ 0.7 x Vdd Oscillation; VIL ≤ 0.3 x Vdd High Impedance	
Jitter RMS 1σ (at 25°C)			8ps typ. - < 40MHz 5ps typ. - ≥ 40MHz		15ps typ. - < 40MHz 8ps typ. - ≥ 40MHz	
Aging (at 70°C)	± 5ppm max. first year / ± 2ppm typ. per year thereafter					

(\*) Available in 2.5Vdc (N) or 1.8Vdc (R)

Z Output logic can drive up to 200 pF load with typical 6ns rise & fall times (tr, tf)  
 ECL, PECL, LVPECL are available. Please contact Q-Tech for details.

**Package Outline and Pin Connections**

Dimensions are in inches (mm)

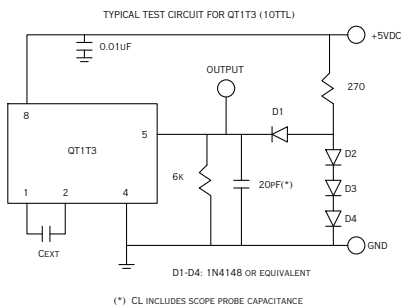


QT #	Conf	Vcc	GND	Case	Output	E/D or N/C	Ext. Cap	Equivalent MIL-PRF-55310 Configuration
QT1	A	8	4	4	5	3	1 & 2	/09 = QT1T /12 = QT1C
QT2	B	12	6	6	5	3	9 & 10	N/A
QT3	C	8	4	4	5	3	1 & 2	/10 = QT3T /13 = QT3C
QT14	D	8	4	4	5	3	1 & 2	N/A

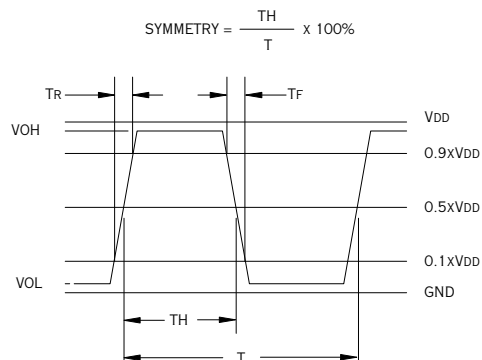
**Package Information**

- Package material (header and leads): Kovar
- Lead finish: Gold Plated – 50μ ~ 80μ inches  
Nickel Underplate – 100μ ~ 250μ inches
- Cover: Pure Nickel Grade A
- Package to lid attachment: Resistance weld
- Weight: 2.0g typ., 4.96g max.

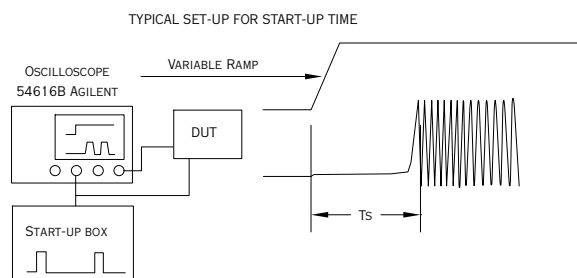
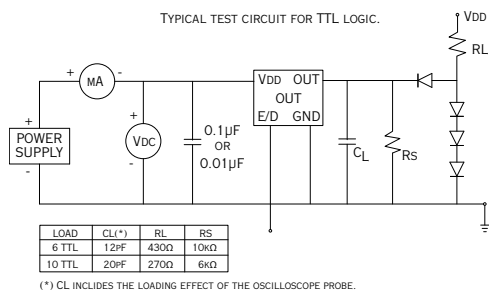
### Test Circuit



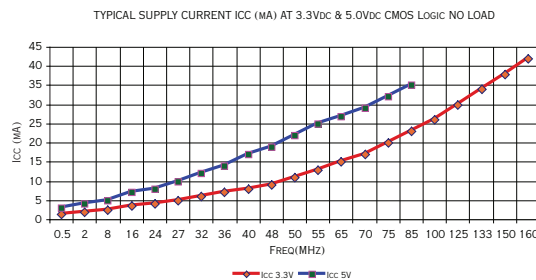
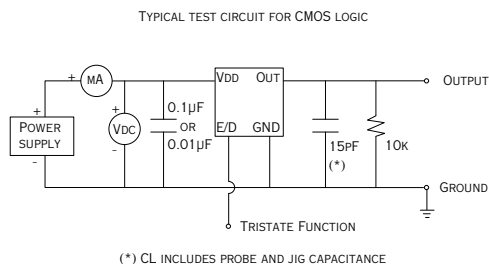
### Output Waveform (Typical)



### Startup Time

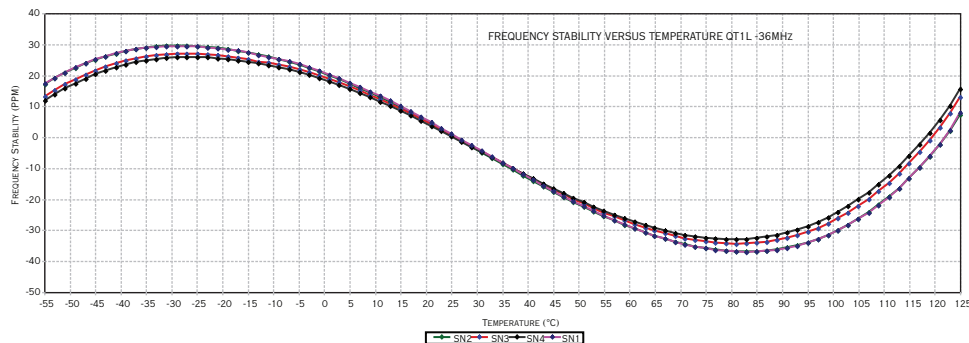


### Supply Current



The Tristate function on pin 1 has a built-in pull-up resistor typical 50kΩ, so it can be left floating or tied to Vdd without deteriorating the electrical performance.

### Frequency vs. Temperature Curve



### Thermal Characteristics

The heat transfer model in a hybrid package is described in figure 1.

Heat spreading occurs when heat flows into a material layer of increased cross-sectional area. It is adequate to assume that spreading occurs at a 45° angle.

The total thermal resistance is calculated by summing the thermal resistances of each material in the thermal path between the device and hybrid case.

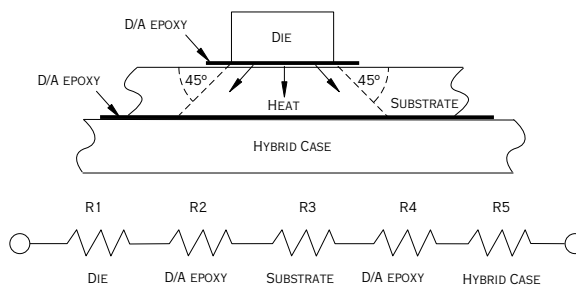
$$RT = R1 + R2 + R3 + R4 + R5$$

The total thermal resistance  $R_T$  (see figure 2) between the heat source (die) to the hybrid case is the Theta Junction to Case (Theta JC) in °C/W.

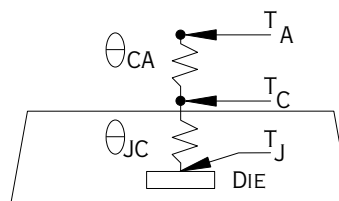
- Theta junction to case (Theta JC) for this product is 30°C/W.
- Theta case to ambient (Theta CA) for this part is 100°C/W.
- Theta Junction to ambient (Theta JA) is 130°C/W.

Maximum power dissipation PD for this package at 25°C is:

- $PD(max) = (T_J(max) - T_A) / \theta_{JA}$
- With  $T_J = 175^\circ C$  (Maximum junction temperature of die)
- $PD(max) = (175 - 25) / 130 = 1.15W$



**(Figure 1)**



$$\theta_{JA} = \theta_{JC} + \theta_{CA}$$

**(Figure 2)**

### Environmental Specifications

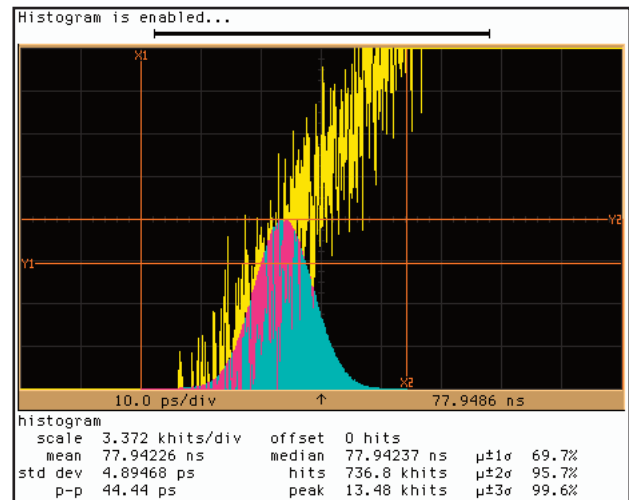
Q-Tech Standard Screening/QCI (MIL-PRF55310) is available for all of our Transistor Outline packages. Q-Tech can also customize screening and test procedures to meet your specific requirements. The Transistor Outline packages are designed and processed to exceed the following test conditions:

Environmental Test	Test Conditions
Temperature cycling	MIL-STD-883, Method 1010, Cond. B
Constant acceleration	MIL-STD-883, Method 2001, Cond. A, Y1
Seal: Fine and Gross Leak	MIL-STD-883, Method 1014, Cond. A and C
Burn-in	160 hours, 125°C with load
Aging	30 days, 70°C
Vibration sinusoidal	MIL-STD-202, Method 204, Cond. D
Shock, non operating	MIL-STD-202, Method 213, Cond. I
Thermal shock, non operating	MIL-STD-202, Method 107, Cond. B
Ambient pressure, non operating	MIL-STD-202, 105, Cond. C, 5 minutes dwell time minimum
Resistance to solder heat	MIL-STD-202, Method 210, Cond. C
Moisture resistance	MIL-STD-202, Method 106
Terminal strength	MIL-STD-202, Method 211, Cond. C
Resistance to solvents	MIL-STD-202, Method 215
Solderability	MIL-STD-202, Method 208
ESD Classification	MIL-STD-883, Method 3015, Class 1HBM 0 to 1,999V
Moisture Sensitivity Level	J-STD-020, MSL=1

**Please contact Q-Tech for higher shock requirements**

### Period Jitter

As data rates increase, effects of jitter become critical with its budgets tighter. Jitter is the deviation of a timing event of a signal from its ideal position. Jitter is complex and is composed of both random and deterministic jitter components. Random jitter (RJ) is theoretically unbounded and Gaussian in distribution. Deterministic jitter (DJ) is bounded and does not follow any predictable distribution. DJ is also referred to as systematic jitter. A technique to measure period jitter (RMS) one standard deviation ( $1\sigma$ ) and peak-to-peak jitter in time domain is to use a high sampling rate (>8G samples/s) digitizing oscilloscope. Figure shows an example of peak-to-peak jitter and RMS jitter ( $1\sigma$ ) of a QT1ACD-40MHz, at 5.0Vdc.



RMS jitter ( $1\sigma$ ): 4.89ps

Peak-to-peak jitter: 44.4ps

### Phase Noise and Phase Jitter Integration

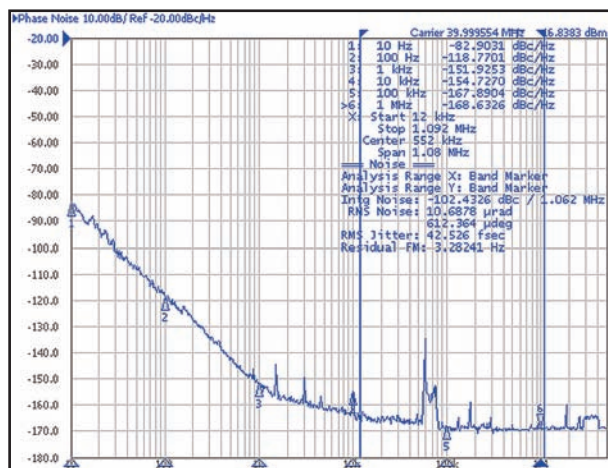
Phase noise is measured in the frequency domain, and is expressed as a ratio of signal power to noise power measured in a 1Hz bandwidth at an offset frequency from the carrier, e.g. 10Hz, 100Hz, 1kHz, 10kHz, 100kHz, etc. Phase noise measurement is made with an Agilent E5052A Signal Source Analyzer (SSA) with built-in outstanding low-noise DC power supply source. The DC source is floated from the ground and isolated from external noise to ensure accuracy and repeatability.

In order to determine the total noise power over a certain frequency range (bandwidth), the time domain must be analyzed in the frequency domain, and then reconstructed in the time domain into an rms value with the unwanted frequencies excluded. This may be done by converting  $L(f)$  back to  $S\phi(f)$  over the bandwidth of interest, integrating and performing some calculations.

Symbol	Definition
$\int L(f)$	Integrated single side band phase noise (dBc)
$S\phi(f) = (180/\pi) \times \sqrt{2} \int L(f) df$	Spectral density of phase modulation, also known as RMS phase error (in degrees)
RMS jitter = $S\phi(f) / (f_{osc} \cdot 360^\circ)$	Jitter (in seconds) due to phase noise. Note $S\phi(f)$ in degrees.

The value of RMS jitter over the bandwidth of interest, e.g. 10kHz to 20MHz, 10Hz to 20MHz, represents 1 standard deviation of phase jitter contributed by the noise in that defined bandwidth.

Figure below shows a typical Phase Noise/Phase jitter of a QT1ACD10M, 5.0Vdc, 40MHz clock at offset frequencies 10Hz to 5MHz, and phase jitter integrated over the bandwidth of 12kHz to 1MHz.



QT1ACD10M, 5.0Vdc - 40MHz